

Model:KABYLAKE-U AIO  
PCB Version:SB  
PCB Number:15107  
PCB P/N:  
SCH Version:  
ECO# number :

PAGE	TITLE	
01	Cover Page	
02	Block Diagram	
03	Reserved	
04	CPU(JTAG/CPU SIDE BAND)	
05	CPU(DDR4)	
06	CPU_(CFG)	
07	CPU(POWER)	
08	CPU(DISPLAY)	
09	Reserved	
10	CPU(POWER CAP1)	
11	CPU(POWER CAP2)	
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17	CPU(ACPI/CLK)	
18	CPU(SPI/SMBUS/LPC)	
19	CPU(HDA)	
20	CPU(GPIO/UART/SPI/I2C)	
21	CPU(POWER)	
22	CPU(RSVD)	
23	CPU(VSS)	
24	EC_KBC NPCE285	
25	Flash ROM/RTC	
26	FAN CIRCUITS/HOLE/THER	
27	AUDIO ALC3661	
28	AMP_ALC1302	
29	MIC/SPEAKER/AUDIO JACK	
30	Reserved	
31	LAN RTL8106E	
32	RJ45+Transformer	
33	CardReader CONN	
34	USB2.0 CONN	
35	USB3.0 CONN	
36	TPM	
37	USB Charger	
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40	RUN PWR/USB PWR	
41	DSW POWER CTL	
42	DC IN/BATT CONN	
43	DDR4 POWER EN & SEQ	
44	CHARGER(BQ24727)	
45	RT6575D 5V/3D3V	
46	NCP81206MN CPU_VCORE(1/3)	
47	NCP81206MN CPU_VCORE(2/3)	
48	NCP81206MN CPU_VCCGT(3/3)	
49	(Reserved)	
50	NCP81253MN CPU_VCCSA	
51	MEM&VTT_RT8231A_1D2V	
52	1D0V/VCCIO/2D5V_VPP	
53	LDO APL5930KAI 1D8V	
54	Reserved	
55	SCALAR	
56	HDMI_IN	
57	HDMI_OUT	
58	Panel Control	

[illegible]

## BOM Configuration

```
(R) : UNMOUNT
```

(G) : GPU

(U) : UMA

(T ) : TOUCH

```
(C ) : REAR IO CONN(non-battery)
```

```
(X ) : XDP & DEBUG USE(REMOVE AT 1A)
```

```
(D):DEBUG USE(REMOVE AT MP)
```

(B) : BATTERY

(E ) : 10/100 LAN

```
(L ) :Giga LAN
```

### PCB BOARD SIZE

6 Layers

*185mm X 230mm*

## SA BUILD

## Intel Kabylake-U Platform

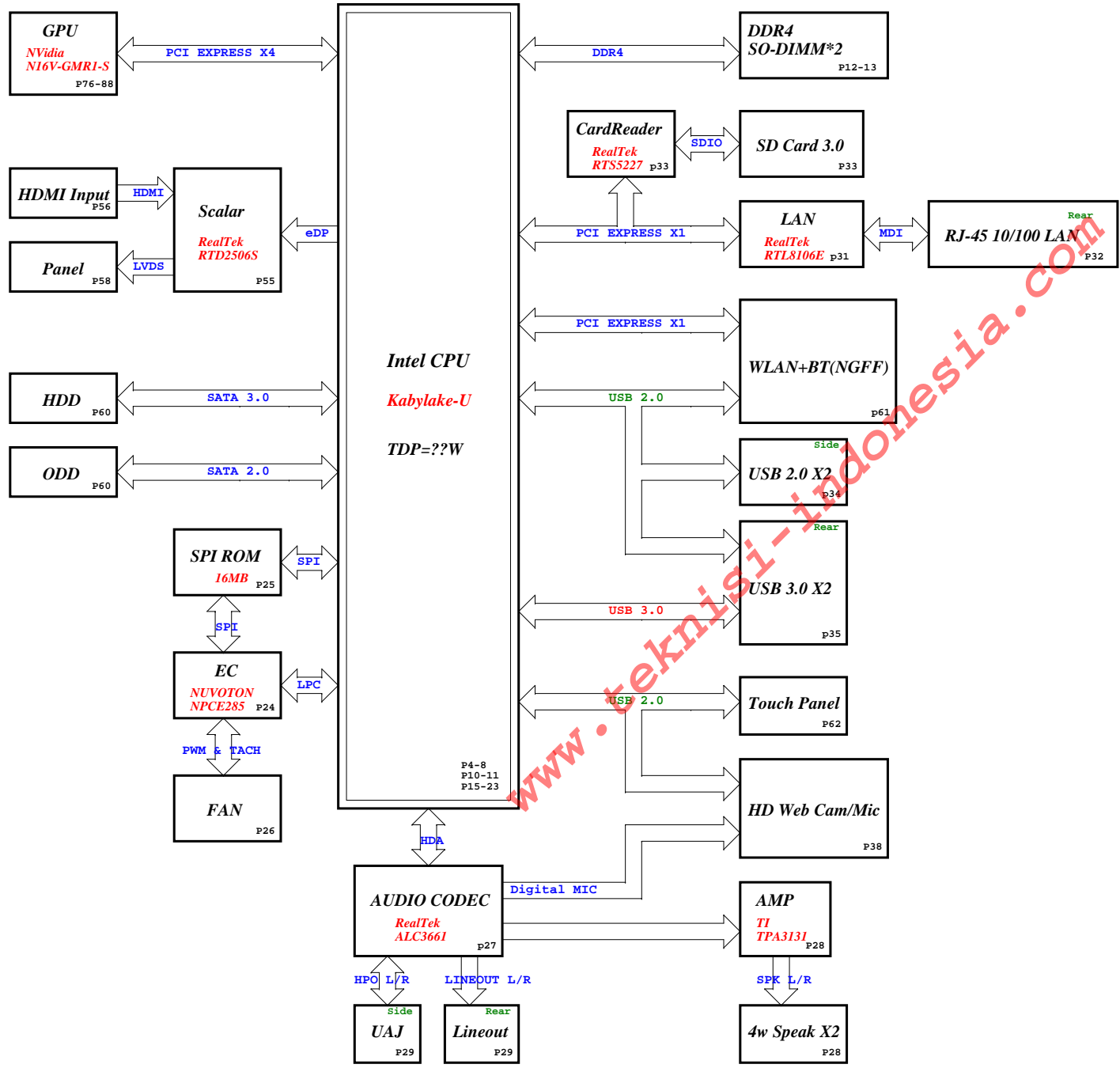
LAN : Gb LAN RTL8111H

**AUDIO: ALC3661**


EC:

Project Name: Jasmine-KBL-U AIO  
Project Code: 3PD05F010001  
PCB Version: SA  
PCB Number :15107

PCB BOARD SIZE  
185mm X 230mm  
6 Layer



CHARGER		P44
BQ24727RGRR		
INPUTS	OUTPUTS	
DC_19V	DCBATOUT BT+	
SYSTEM DC/DC		P45
RT6575DGQW		
INPUTS	OUTPUTS	
DCBATOUT	V_5P0_A V_3P3_A	
CPU Core Power		P46-50
NCP81206MNTXG		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE 1V_VCCGT 1V_VCCSA	
DDR4 Power		P51
RT8231AGQW		
INPUTS	OUTPUTS	
DCBATOUT	DDR_VDDQ MEM_VTT	
CPU1V and switch		P52
RT8237CZQW		
INPUTS	OUTPUTS	
DCBATOUT 1D0V_S5	1D0V_S5 1V_VCCIO	
SYSTEM 1D8V		P53
APL5930KA1		
INPUTS	OUTPUTS	
SB3V	1D8V_S5	
PANEL BL POWER		P59
OZ554ALN		
INPUTS	OUTPUTS	
DCBATOUT	VOUT_INV	
GPU CORE POWER		P88
NCP81172MNTXG		
INPUTS	OUTPUTS	
DCBATOUT	+V_VGA_CORE	
GPU POWER		P86
INPUTS	OUTPUTS	
DCBATOUT DDR_VDDQ	+V_1P35_VGA +V_1P05_VGA	
SWITCH		P41-42
INPUTS	OUTPUTS	
V_5P0_A V_3P3_A V_5P0_A V_3P3_A	VCC VCC3 SB5V SB3V	
PCB LAYER		
L1:TOP		
L2:GND		
L3:SIGNAL/POWER		
L4:SIGNAL/POWER		
L5:GND/POWER		
L6:BOTTOM		



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Title

002\_Block Diagram

Size

C

Document Number

Rosa\_KBL-U AIO

Rev

SB

Date:

Thursday, June 23, 2016

Sheet

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of

105

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<Core Design>SB-010



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Title

**003\_ (Reserved)**

Size  
A

Document Number

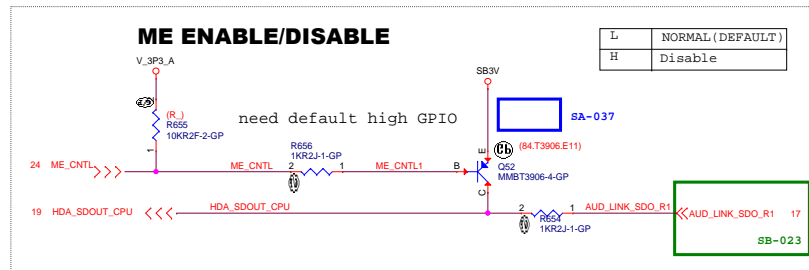
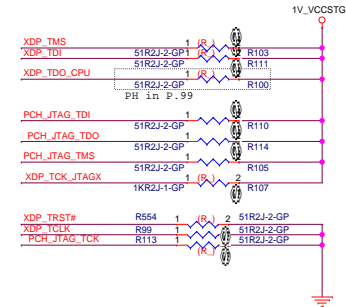
**Rosa\_KBL-U AIO**

Rev  
**SB**

Date: Thursday, June 23, 2016

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#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm  
#544669 Rev0.52:  
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm



# Main Func = CPU

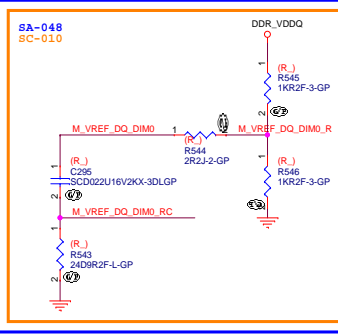
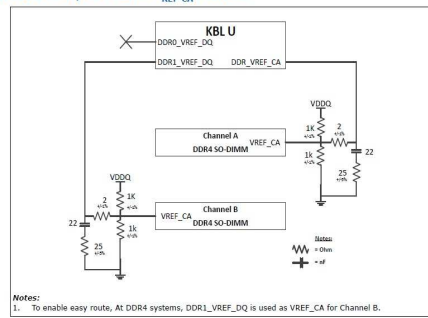
## DDR4 ball type: Non-Interleaved Type

12 M\_A\_DQ[63:0] <<>  
12 M\_A\_A[16:0] <<>  
12 M\_A\_DQS\_DN[7:0] <<>  
12 M\_A\_DQS\_DP[7:0] <<>

13 M\_B\_DQ[63:0] <<>  
13 M\_B\_A[16:0] <<>  
13 M\_B\_DQS\_DN[7:0] <<>  
13 M\_B\_DQS\_DP[7:0] <<>



Figure 4-49. KBL U DDR4/-RS SODIMM VREF\_CA Overview



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File: 005\_CPU(DDR4)(NEW)

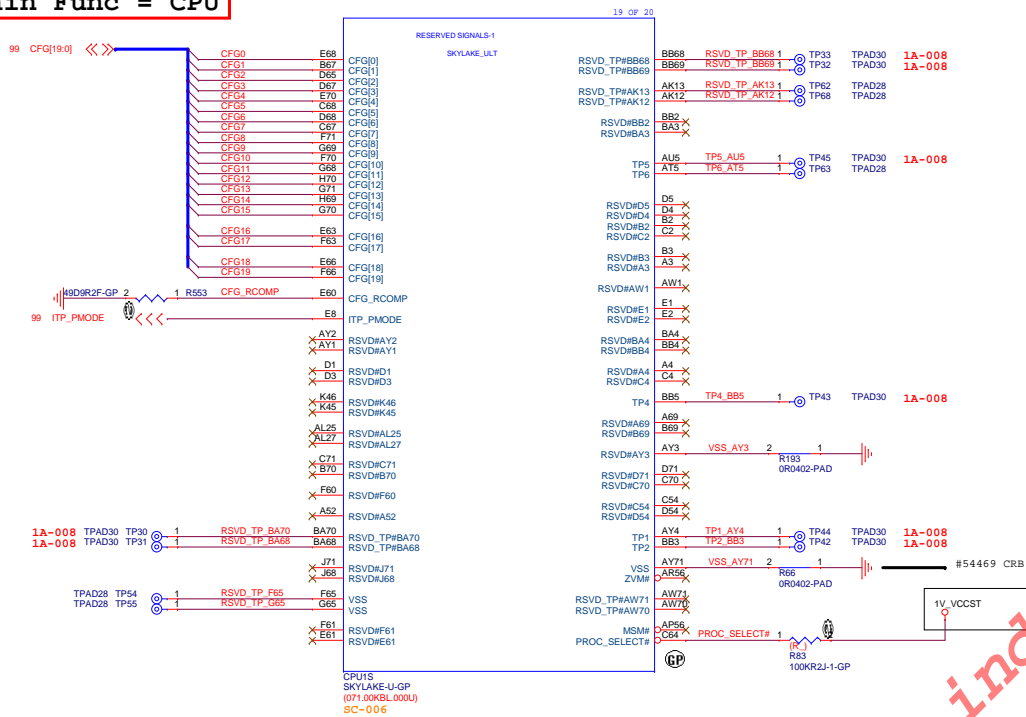
Size: C

Document Number: Rosa\_KBL-U AIO

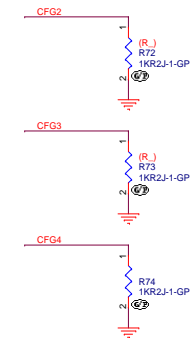
Date: Thursday, June 23, 2016

Sheet: 5 of 105

Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX_ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)

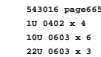
DISPLAY PORT PRESENCE STRAP	
CFG[4]	<p>0 : ENABLED            An external Display Port device is connected to the Embedded Display Port.</p> <p>1 : DISABLED (Default)            No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.</p>

```
SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*
```

### Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

+V\_EOPIO\_VR and +V\_EDRAM\_VR powere source from 1D0V\_S0



## Main Func = CPU

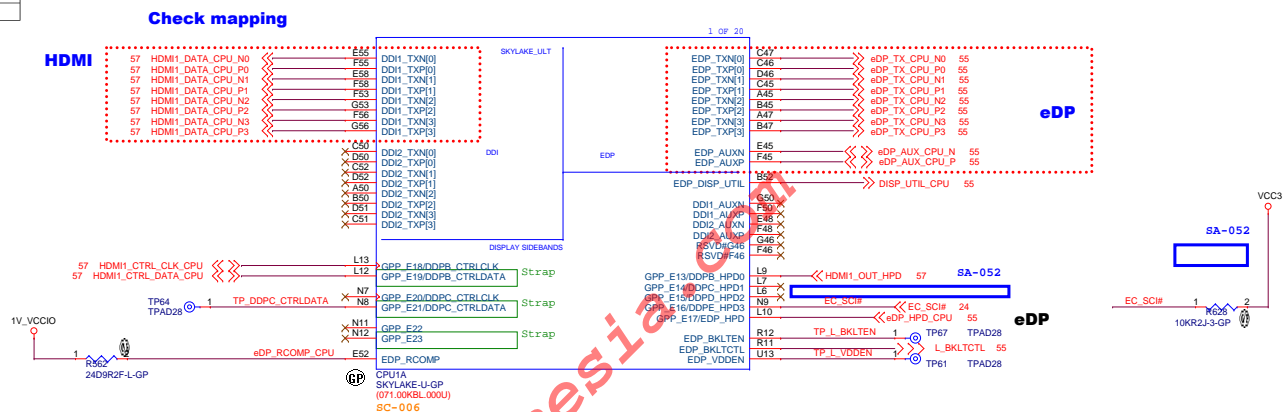
Table 5-10. DDI Disabling and Termination Connections

Pin Name	Recommendation
DDPB_AUXP DDPB_AUXP	No Connect
DDPB_AUXN DDPB_AUXN	No Connect
DDPB_HPD DDPB_HPD	No Connect
DDI1_TXP[3:0] DDI2_TXP[3:0]	No Connect
DDI1_TXN[3:0] DDI2_TXN[3:0]	No Connect
DDPB_CTRLCLK DDPB_CTRLDATA	No Connect
DDPC_CTRLCLK DDPB_CTRLDATA	No Connect

### Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



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Title: 008\_CPU(DISPLAY)  
Size: C Document Number: Rosa\_KBL-U Aio Rev: SB  
Date: Thursday, June 23, 2016 Sheet: 8 of 105



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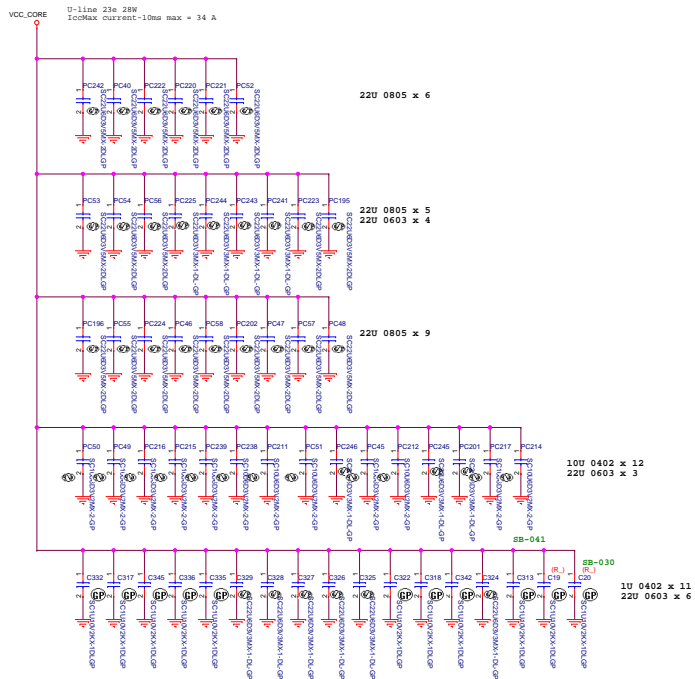


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Title		
009_(Reserved)		
Size	Document Number	Rev
B	Rosa_KBL-U AIO	SB
Date:	Thursday, June 23, 2016	Sheet 9 of 105

Main Func = CPU

## CORE CAP follow Cap\_Sorting list



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Taippei Hsien 321, Taiwan, R.O.C.

File  
010\_CPU(POWER CAP1)

Size  
Com Rosa\_KBL-U AIO

Rev  
SB

Date Thursday, June 28, 2018 Sheet 10 of 16

- **VCC<sub>prim\_core</sub>** Power well and **VCC<sub>SP1</sub>** power supply wells will be required to be powered by the **1.0 V and 3.3 V (or 1.8 V)** power well, respectively.
- Support for power sequencing signals as described in the Skylake Platform Intel® Management Engine (Intel® ME) and Embedded Controller (EC) Interaction - Product Specification.

```
U-line 23e 28W
IccMax current-10ms max[A] = 67 A
```

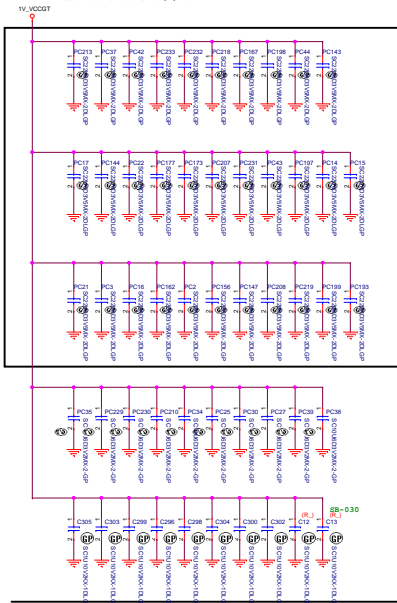
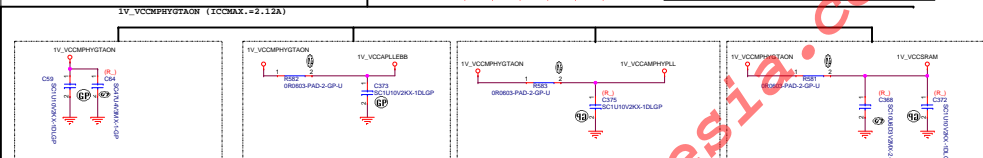
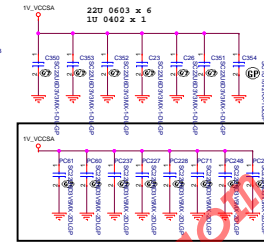
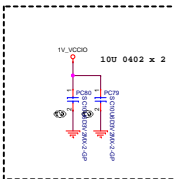
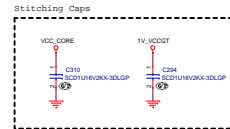
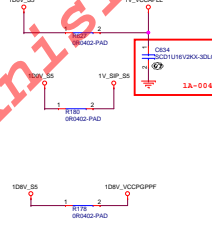
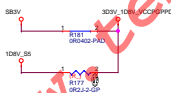
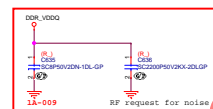
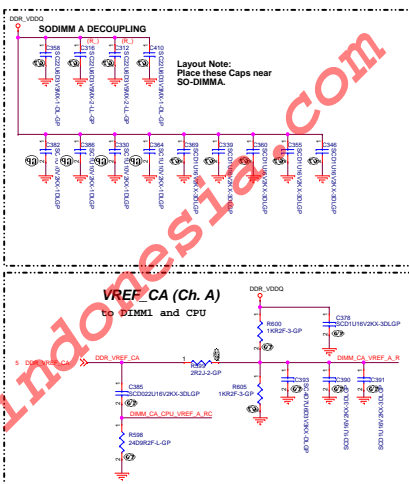
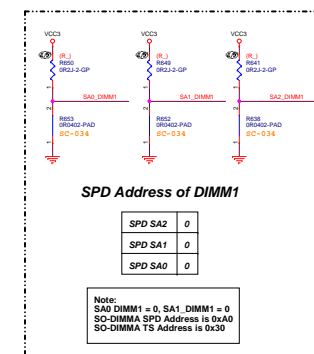


Diagram showing the connections for pins 1 through 15 of the 15-pin connector. The connections are as follows:

- Pin 1: 12V\_5S
- Pin 2: 1V\_VCC24N7
- Pin 3: 1V\_VCC24T8T
- Pin 4: 1V\_VCC9PM
- Pin 5: 1V\_VCC9PM
- Pin 6: 1V\_VCC24T8T
- Pin 7: 1V\_VCC24T8T
- Pin 8: 1V\_VCC24T8T
- Pin 9: 1V\_VCC24T8T
- Pin 10: 1V\_VCC24T8T
- Pin 11: 1V\_VCC24T8T
- Pin 12: 1V\_VCC24T8T
- Pin 13: 1V\_VCC24T8T
- Pin 14: 1V\_VCC24T8T
- Pin 15: 1V\_VCC24T8T

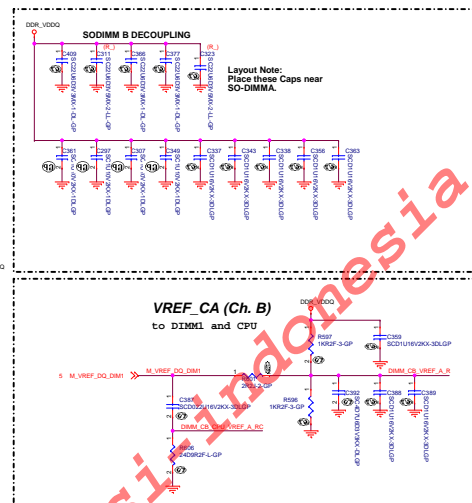
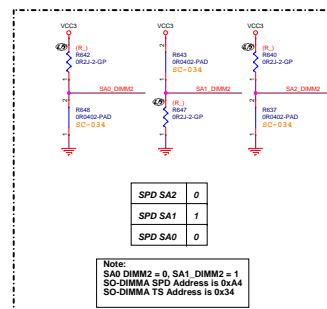
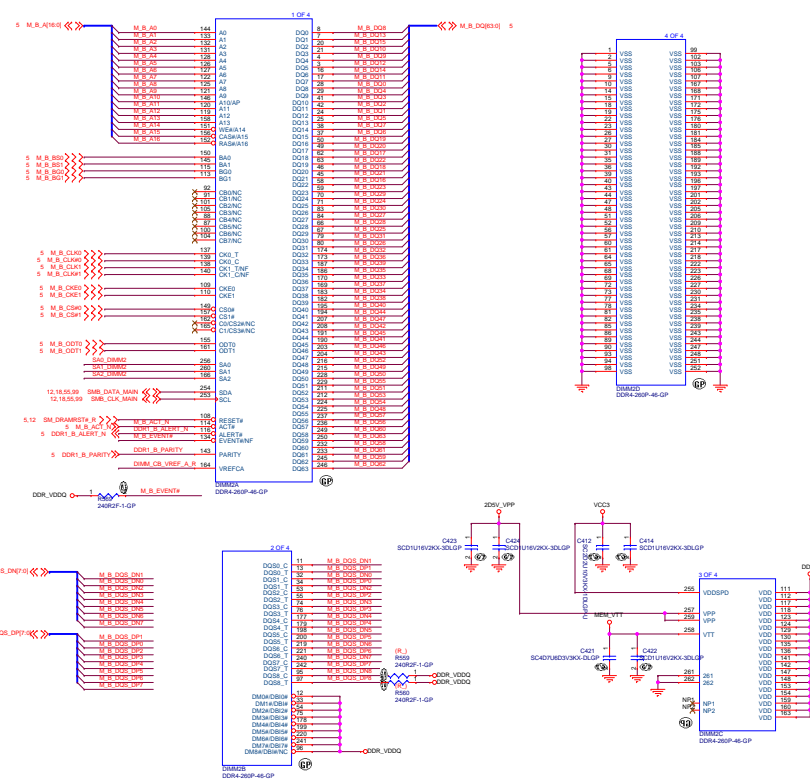
```
1V_VCOGTUS(VeeGTX) (ICCMAX.=18A)
```

[illegible]



SPD Address Table			
SMBus 0			
Device	8-bit Address(hex)		
DIMM A0	Memory Address:0x00	SA1=0;SA0=0	
DIMM A1	Memory Address:0x01	SA1=0;SA0=0	
DIMM B0	Memory Address:0x02	SA1=1;SA0=0	
DIMM B1	Memory Address:0x03	SA1=1;SA0=0	
1	0	1	0
0	0	0	0


Note:0' 3-7 bit as default



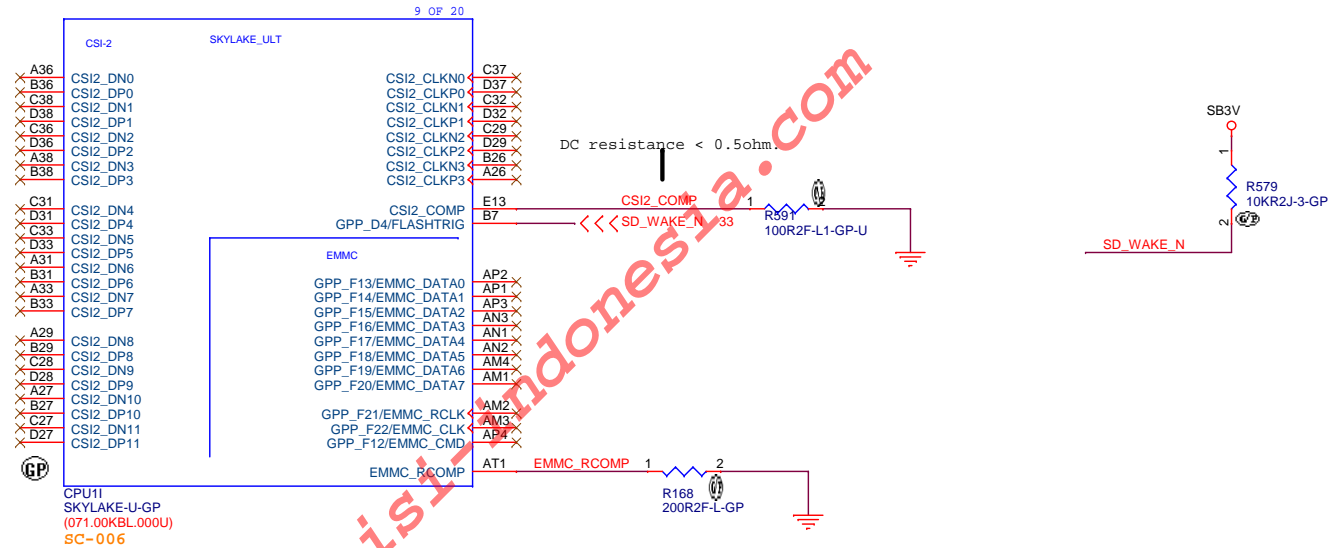
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Title <b>014_ (Reserved)</b>		
Size A4	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016		Sheet 14 of 105

Main Func = PCH



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Title <b>015_CPU(CSI2/EMMC)</b>		
Size B	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
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\*SATA Port 1 can be configured to PCIe Port 8 or 11  
Not all ports are available on all SKUs



SKL	PCIe Link Config	PCI Express Lanes										
		1	2	3	4	5	6	7	8	9	10	11
U	1x4	Port1			Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11
	1x2 + 2x1	Port1		Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11
	1x4	Port1			Port5				Port9			
Y	2x2			Port3				Port7				
	1x2 + 2x1	Port1		Port3	Port4	Port5	Port6	Port7	Port8			
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8			
	1x2									Port9		
	2x1									Port9 + Port10		

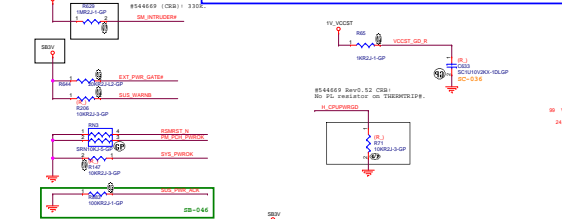
U802 Port6	U802 Port6
U802 Port7	U802 Port7
U802 Port8	NC
U802 Port9	NC
U802 Port10	NC

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

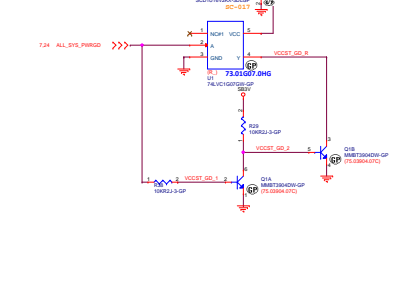




**Main Func = PCH**

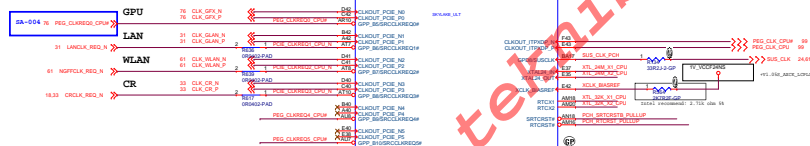
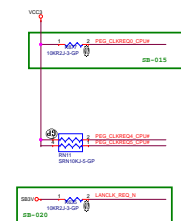


VCCST\_PWRGD / HWM201:



### CLK OUT Table

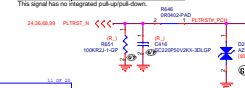
Pair	Device
0	Reserved
1	SSD(RQ1#)
2	LAN(RQ2#)
3	WLAN(RQ3#)
4	Reserved
5	Reserved



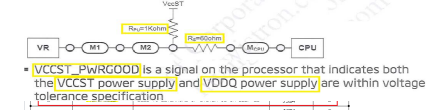
**GPP\_A13-15 pin(LPC/eSPI):**

**PCH strap pin:**At which pinout for SKL:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable High = Enable (default) ★



## VCCST\_PWRGOOD



4	MSB31_30_N	WHEN ASSERTED (0) SYSTEM IS IN HS	2304	5
5	MSB31_30_N	WHEN ASSERTED (0) SYSTEM IS IN HS	2304	11
8	MSB31_30_N	WHEN ASSERTED (0) INTEL MC IS HOFF	2304	24
7	MSB31_30_N	USED TO DETERMINE IF SYSTEM IS IN DEEP S4/HS	2304	31

14	GN0	Ground for SYS_RESET#
15	SUP_S0#	When asserted (0) system is in deterministic idle state
16	NC	No Connection
17	NC	No Connection
18	NC	No Connection

RATLOW#:  
Pull-up required even if not implemented.

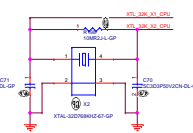
PASSWORD CLEAR



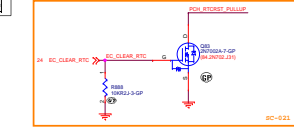
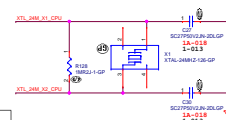
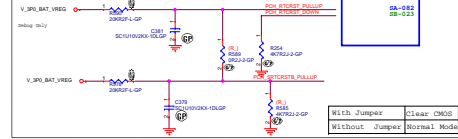
APS\_Pin3&7:

#543016 Rev0.7

1. VCCST\_PMSGD is only 1.0 V tolerant.
2. VCCST\_PMSGD must go low during Sx per states, regardless of the voltage level of VCCST.



**CLEAN-CMOS**



		Jumper on	Jumper off
1	2	Clear CMOS	NORMAL (DEFAULT)
3	4	NORMAL (DEFAULT)	CLEAR PASSWORD
5	6	ME Disable	NORMAL (DEFAULT)

**PCH strap pin:**

**PCH strap pin:**

DCN Prim

5V

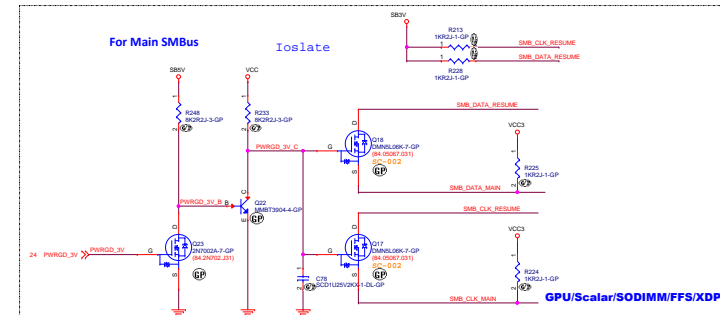
R199  
1KΩ

R185  
1KΩ

PCH strap pin:

TLS Confidentiality

Figure 1: Block diagram of the system architecture. The diagram shows a central 'CPU' block connected to several peripheral components. At the top, a 'GPP\_C2/SMBALERT# 1' line connects to a '10KQ2-1-GP' component. To the right, a 'CPU' block is connected to a '10KQ2-3-GP' component. Below the CPU, a 'GPP\_B03/SMB1ALERT# 1' line connects to a '10KQ2-3-GP' component. At the bottom, a 'LPC\_CLKRUN CPU 1' line connects to a 'BKQ2F-1-GP' component. A 'CPU' block is also shown at the bottom right, connected to the 'BKQ2F-1-GP' component. A 'CPU' block is also shown at the top right, connected to the '10KQ2-1-GP' component.

[illegible]

Main Func = PCH

#### PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs

#### DMIC Table

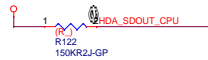
Pair	Device
0	DMIC Port1
1	DMIC Port2

#### PCH strap pin:

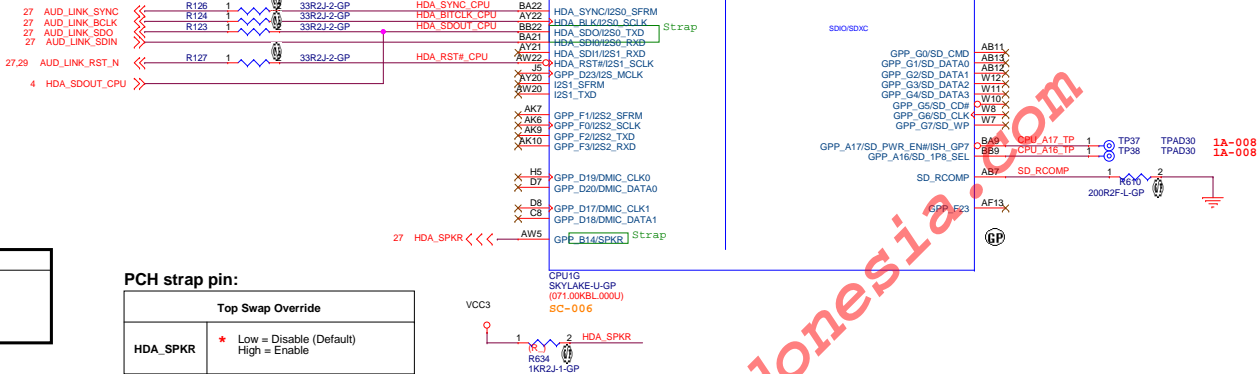
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable

The internal pull-down is disabled after PLTRST# deasserts

SD3V\_1D8V\_VCHDA



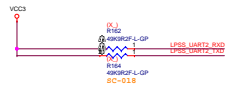
#### AUDIO



Main Func = PCH

Need to confirm!!

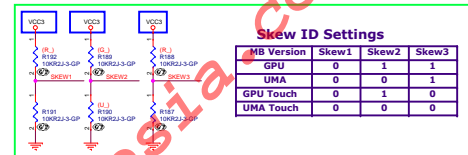
Touch Pad/AUD256



(SD04543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(SD04543016) If the UART/GPIO functionality is also not used, the signals can be safely be no-connect.

Sensor 548926:

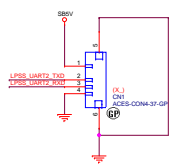


Skew ID Settings

MB Version	Skew1	Skew2	Skew3
GPU	0	1	1
UMA	0	0	1
GPU Touch	0	1	0
UMA Touch	0	0	0

Intel has removed BNC2 controller from BSL2 and proposed to use USB/DART Muxing for Win7 debug.

Pin height 2.5mm



PCH strap pin:

Boot BIOS Strap Bit BBS  
Boot BIOS Destination  
• Low = GPU (Default)  
• High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PE or PL

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**Main Func = PCH**

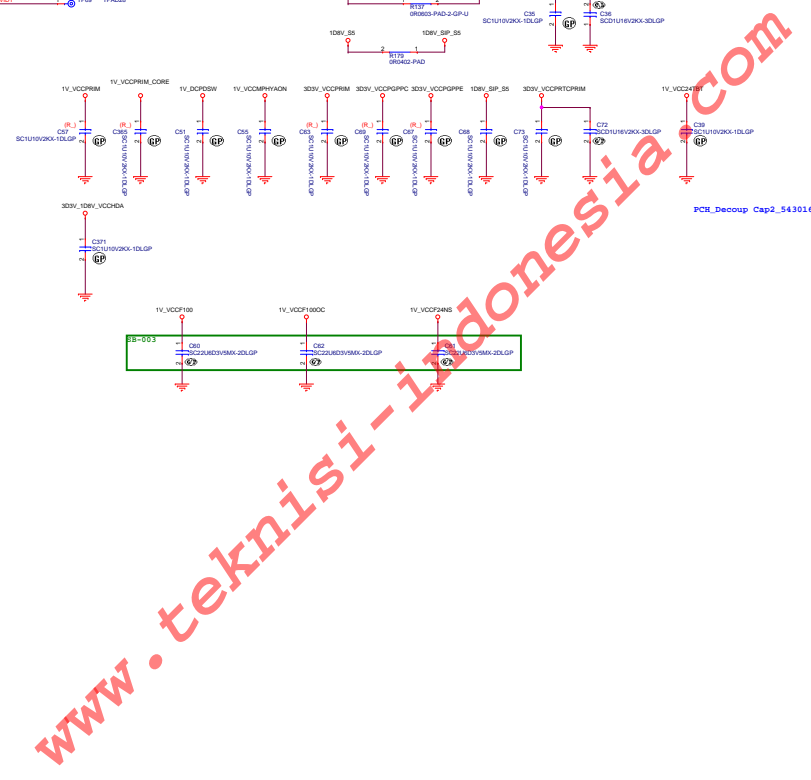


Table 55-8. Decoupling and Power Connection Requirements for SKL U PCH (Sheet 2 of 2)

Voltage Supply	Area	PCB Rising plane size	Value	Size	Quantity	Placement type (x/Runway / Edge)	Place capacitor(s) near ball(s)
V1.0A / V2.4A	VccPRIM	AK20	-	-	-	-	-
V3.3A	VccPRIM	V19, A121	1 uF	0402	1	E (<3 mm)	V19 (Note 1)
	VccPGPPA	AG15	1 uF	0402	1	E (<3 mm)	AG15 (Note 1)
	VccPGPPE	T16	1 uF	0402	1	E (<10 mm)	T16 (Note 1)
	VccPGPP	T16	1 uF	0402	1	E (<10 mm)	T16 (Note 1)
V3.3A / V1.5A / V1.5A	VccIDA	A119	1 uF	0402	1	E (<10 mm)	A119 (Note 1)
V3.3A / V1.5A	VccSPI	A116	-	-	-	-	-
	VccPGPPA	AK15	-	-	-	-	-
	VccPGPD	V15	-	-	-	-	-
	VccPGGP	AD15	-	-	-	-	-
	VccTRIPRIM	AK17	1 uF	0402	1	E (<3 mm)	AK17
V3.3SDW (3.3V)	VccDSW	AD15, A117	0.1 uF	0402	1	-	-
V3.3BTL (3.3V)	VccRTC	AK19, BB14	1 uF	0402	1	E (<3 mm)	AK19
	VccPGPP	AF16	-	-	-	-	-
V1.8A	VccATS	AA1	1 uF	0402	1	E (<10 mm)	AA1
	DeprRTC	BB10	0.1 uF	0402	1	E (<3 mm)	BB10
PCI Interface VDD	OpDSW	AL1	1 uF	0402	1	E (<3 mm)	AL1

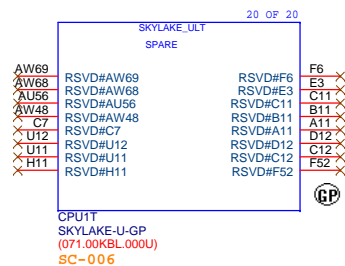
**Note:**

- Placeholder only. Does not need to be stuffed.
- Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" column above to ensure the sharing is optimized.
- Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
- For description of (Runway) and (Edge) decoupling capacitor placement, please refer to "Loop Inductance Reduction Description".

**Note:**

1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to "[Loop Inductance Reduction Decoupling](#)".

Main Func = PCH



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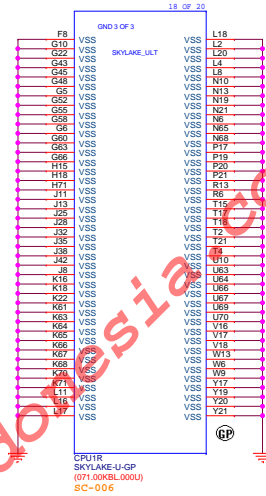
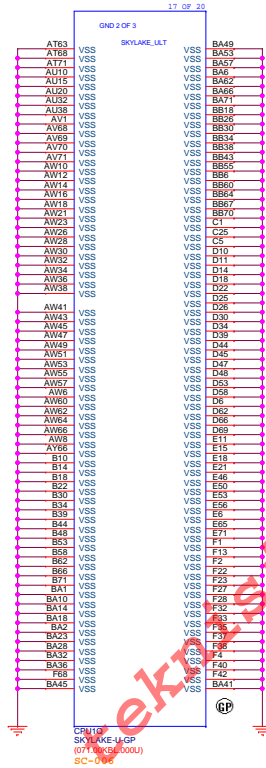
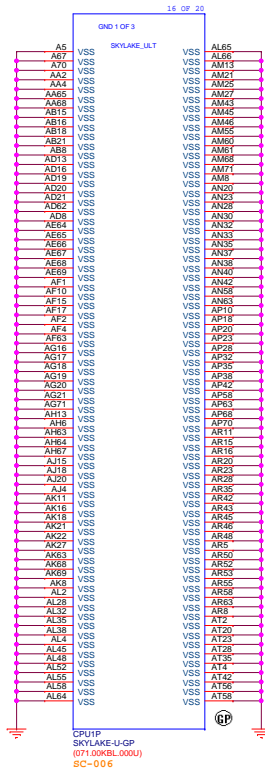
<Core Design>



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Title <b>022_CPU(RSVD)</b>		
Size A3	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016      Sheet 22 of 105		

Main Func = PCH

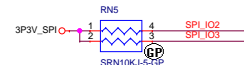






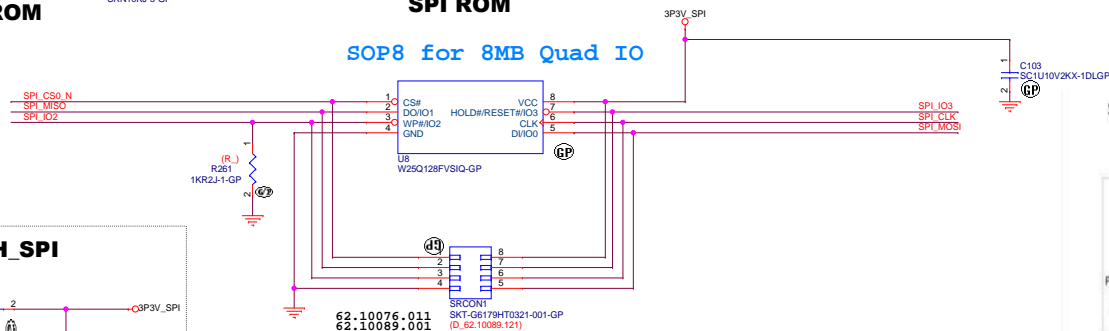
18,24 SPI\_CS0\_N  
18,24 SPI\_MISO  
18 SPI\_IO2  
18 SPI\_IO3  
18,24 SPI\_CLK  
18,24 SPI\_MOSI

## SPI ROM

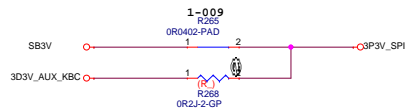


## SPI ROM

### SOP8 for 8MB Quad IO



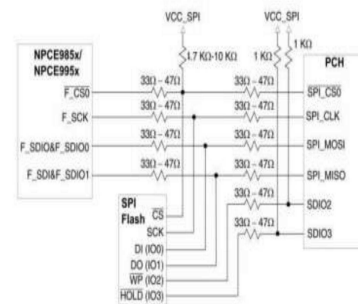
## +V3P3A\_V1P8A\_PCH\_SPI



## SPI ROM

8 MB:  
72.25647.00A - MXIC Quad IO SOP8

### Single SPI shared flash connection (SPI Quad I/O mode)

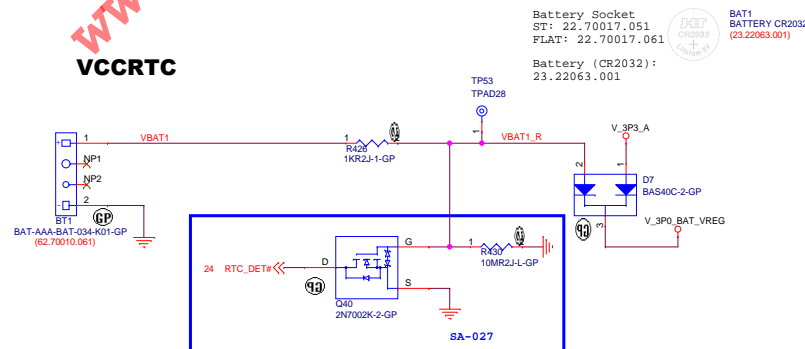


Refer to "NPCE985x/ NPCE995x board design reference guide"

SA-031 SA-036

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## VCCRTC



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Title  
025\_Flash ROM/RTC(NEW)  
Size  
C Document Number  
Rosa\_KBL-U AIO Rev  
SB  
Date: Thursday, June 23, 2016 Sheet 25 of 105

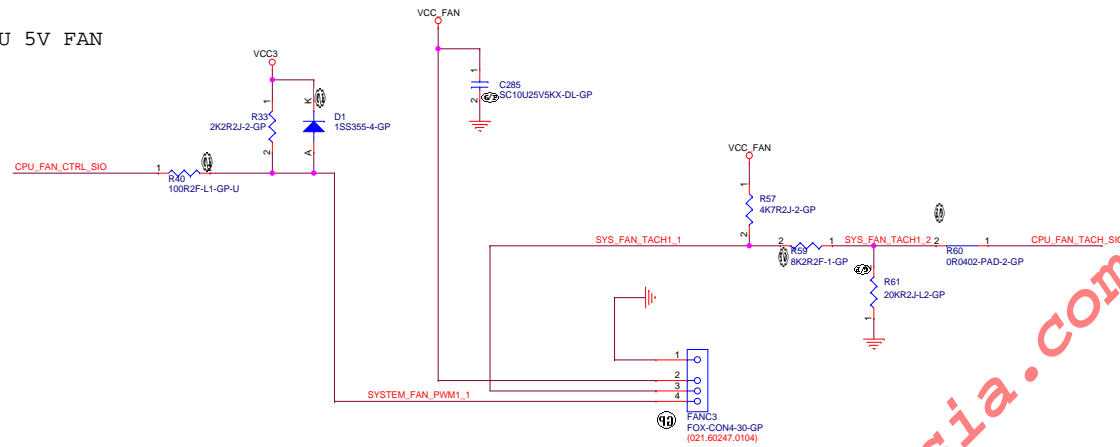
CPU 5V FAN

## SIO FAN CONTROL

```

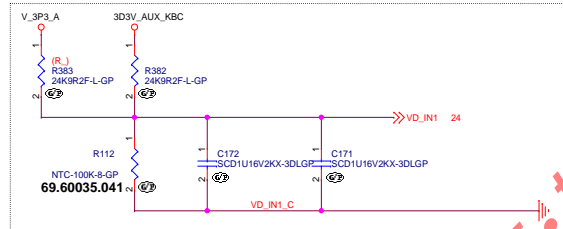
24 CPU_FAN_CTRL_SIO  >>>
24 CPU_FAN_TACH_SIO  <<<

```

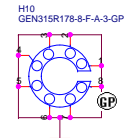
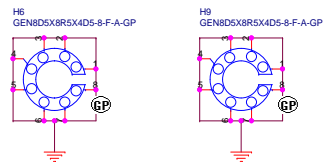
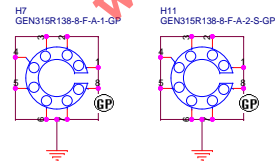
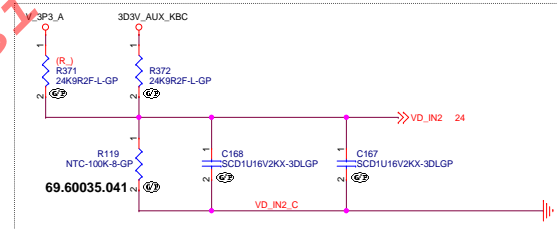


SA-089

VD\_IN1 for VRM thermal sensor



◆ VD\_IN2 for DIMM thermal sensor

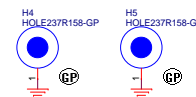


```
0805 modify screw hole to ZZ.0HOLE.011
0731 add screw hole
0730 delete screw hole
0724 add F7 for BOM
0714 change part
```

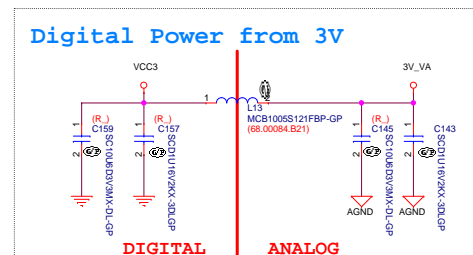
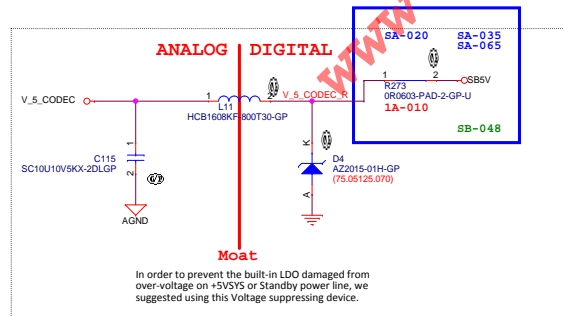
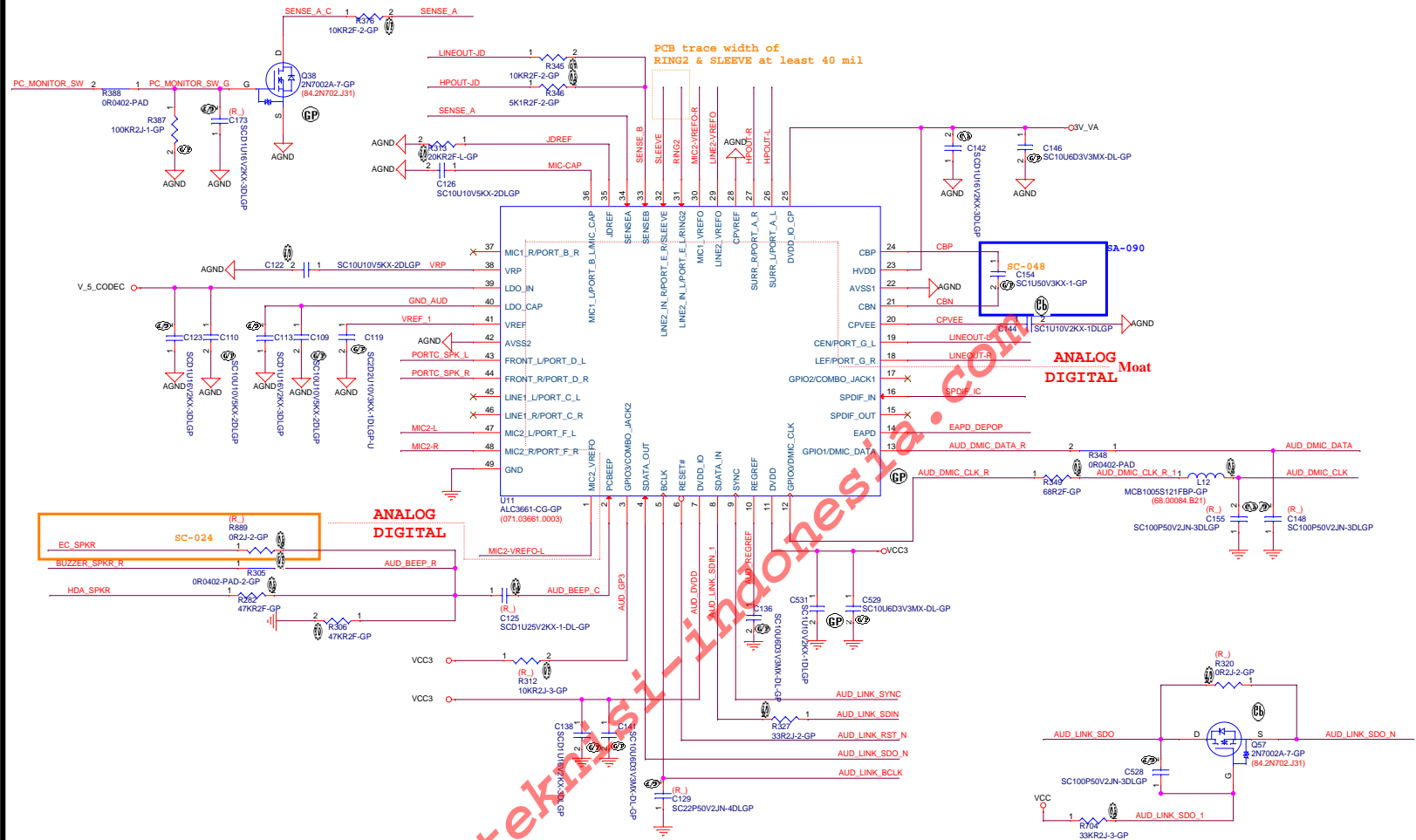
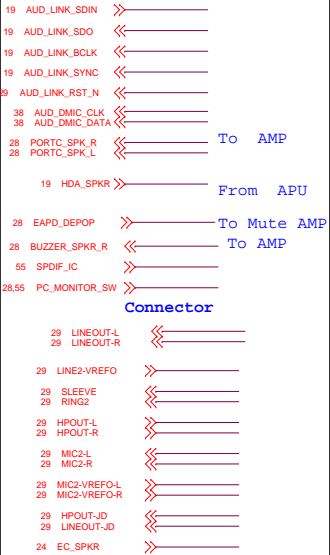
CPU Heatsink screw hole.

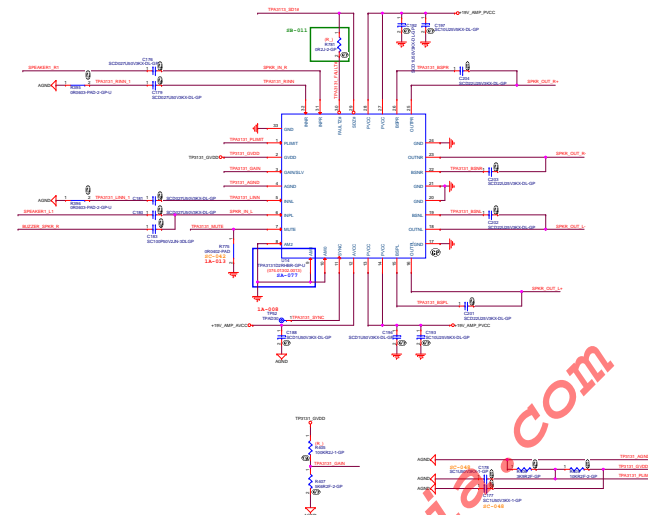


GPU Heatsink screw hole.



## HD\_LINK





eCore Designer	
<b>DELL</b>	<b>Wistron Corporation</b> 217, 8th, Sec. 1, Hsiao-Tsai Rd. No. 1, Shaozhai, Tapei Hsien 207, Taiwan, R.O.C.
File	<b>028_AMP_ALC1302</b>
Doc	Document Number
Rosa	Rosa, KBL-U AIO



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Title

**030\_ (Reserved)**

Size  
A

Document Number

**Rosa\_KBL-U AIO**

Rev

**SB**

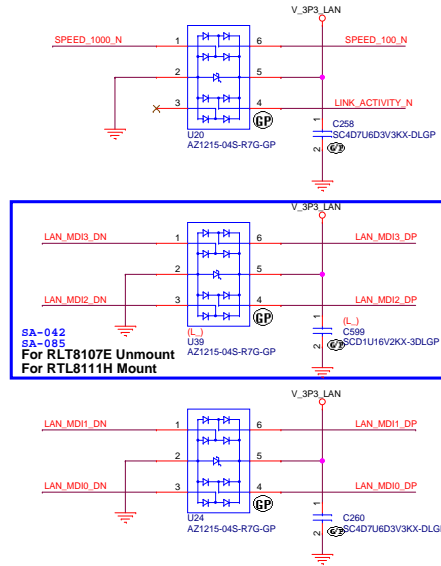
Date: Thursday, June 23, 2016

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31 LAN\_MDIO\_DP  
31 LAN\_MDIO\_DN  
31 LAN\_MD1\_DP  
31 LAN\_MD1\_DN  
31 LAN\_MD2\_DP  
31 LAN\_MD2\_DN  
31 LAN\_MD3\_DP  
31 LAN\_MD3\_DN  
31 LINK\_ACTIVITY\_N  
31 SPEED\_100\_N  
31 SPEED\_1000\_N

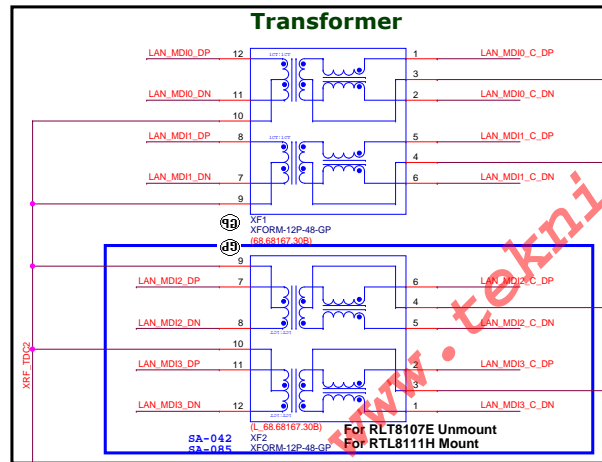
## ESD



For LAN differential signal :



## Transformer



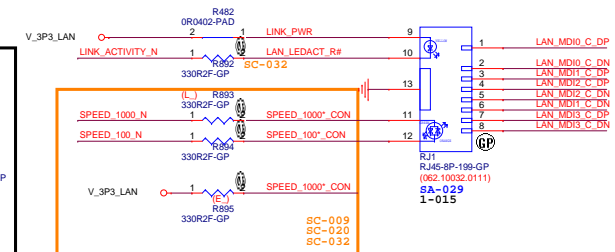
	Giga	100	10
Link	Orange	Green	Green
Act	Yellow	Yellow	Yellow
	Blink	Blink	Blink

Connector

RJ45

## Surge

route 20 mils



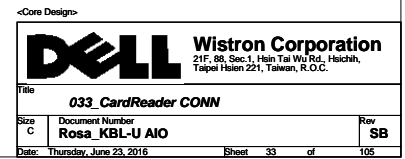
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Size	Document Number	Rev	
C	Rosa_KBL-U AIO	SB	
Date:	Wednesday, July 06, 2016	Sheet	32 of 105

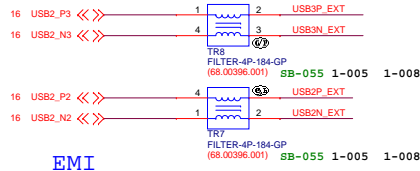


17,18 CRCLK\_REQ\_N <<—  
24 PLTRST\_CR >>—  
17 CLK\_CR\_N >>—  
17 CLK\_CR\_P >>—  
15 SD\_WAKE\_N <<—  
16 PCIE\_RX\_CPU\_N8 >>—  
16 PCIE\_RX\_CPU\_P8 >>—  
16 PCIE\_TX\_CON\_N8 >>—  
16 PCIE\_TX\_CON\_P8 >>—

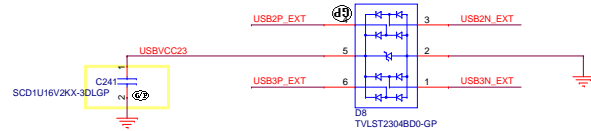


6.34 USB\_OC#2\_3

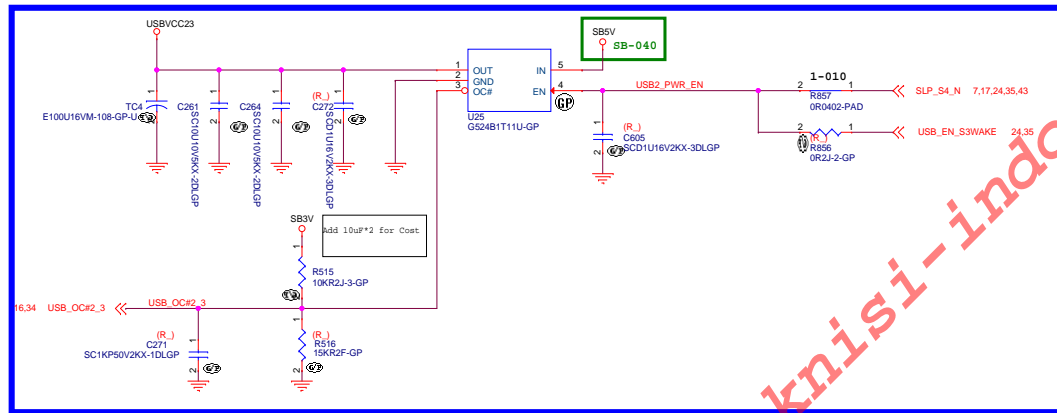
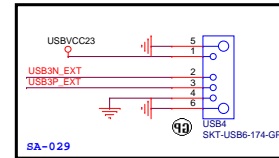
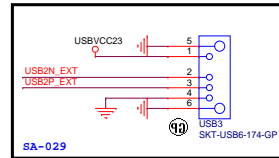
USB



ESD



Rear USB2



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Title: 034\_USB2.0\_CONN

Size: Document Number: Rosa\_KBL-U AIO Rev: SB

Date: Thursday, June 23, 2016 Sheet: 34 of 105

## USB 3.0

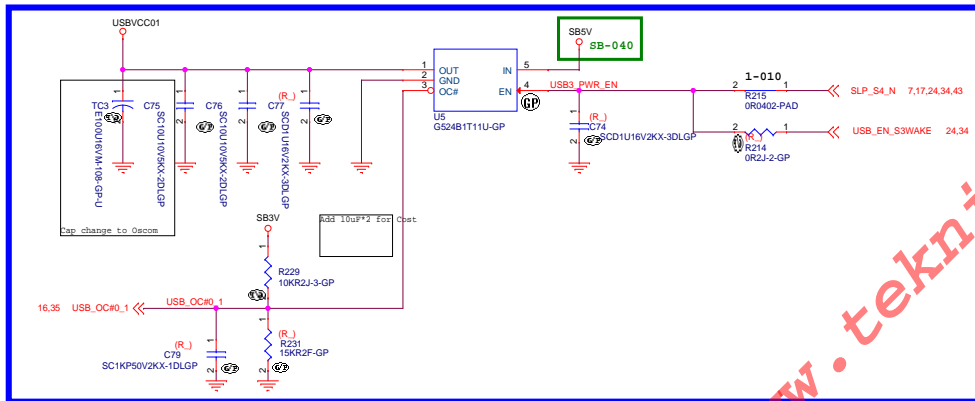
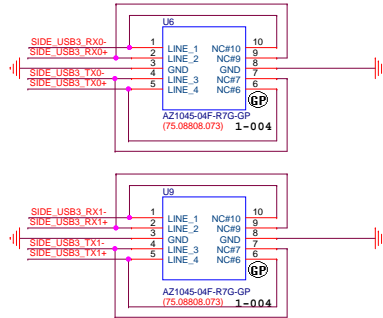
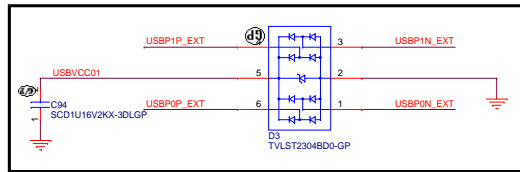
6,35 USB\_OC#0\_1

16 USB30\_RX\_CPU\_N0  
16 USB30\_RX\_CPU\_P0  
16 USB30\_TX\_CPU\_N0  
16 USB30\_TX\_CPU\_P0  
16 USB30\_RX\_CPU\_N1  
16 USB30\_RX\_CPU\_P1  
16 USB30\_TX\_CPU\_N1  
16 USB30\_TX\_CPU\_P1

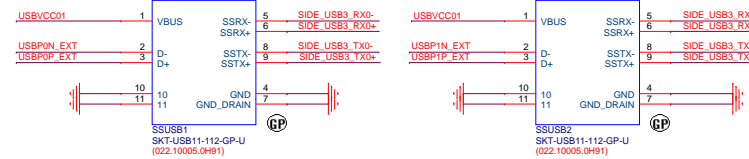
## Richard Check USB Mapping

16 USB2\_N0  
16 USB2\_P0  
16 USB2\_N1  
16 USB2\_P1

## ESD



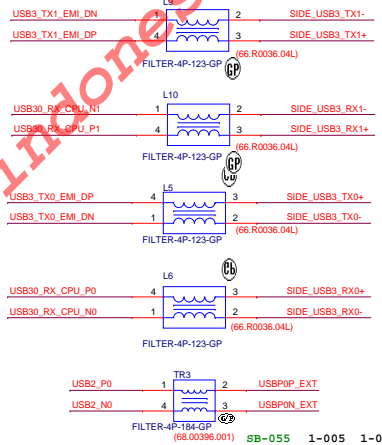
## Side USB 3.0



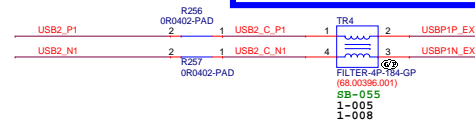
## EMI



## EMI



SA-067



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Title: 035\_USB3.0\_CONN

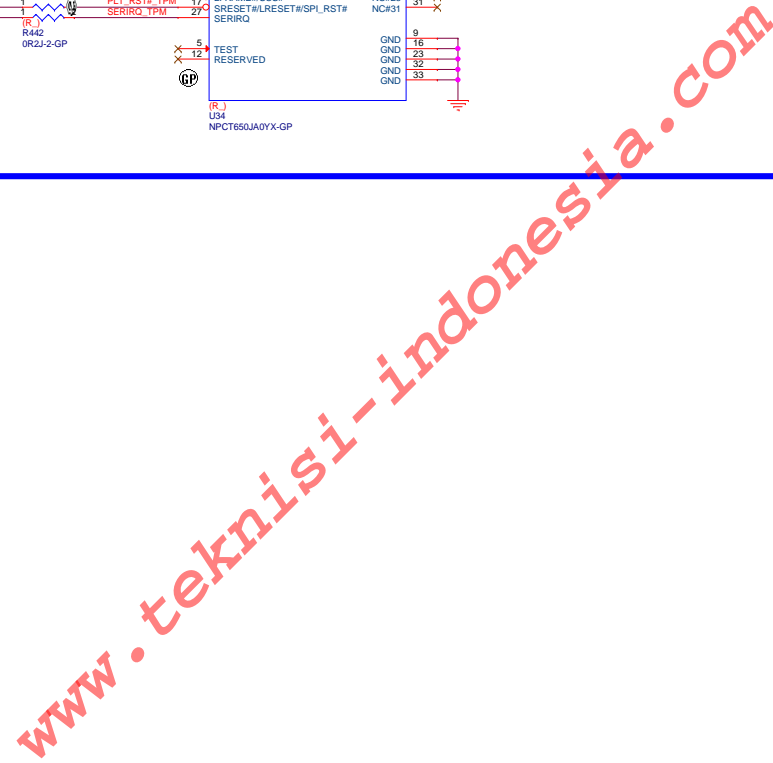
Size: C Document Number: Rosa\_KBL-U AIO Rev: SB

Date: Thursday, June 23, 2016 Sheet: 35 of 105

```


18,24 LPC_CLK1 >>>
18,24,68 L_FRAME_N >>>
17,24,68,99 PLTRST_N >>>
18,24 SERIRQ_CPU >>>
18,24 PM_CLKRUN#_EC >>>

```



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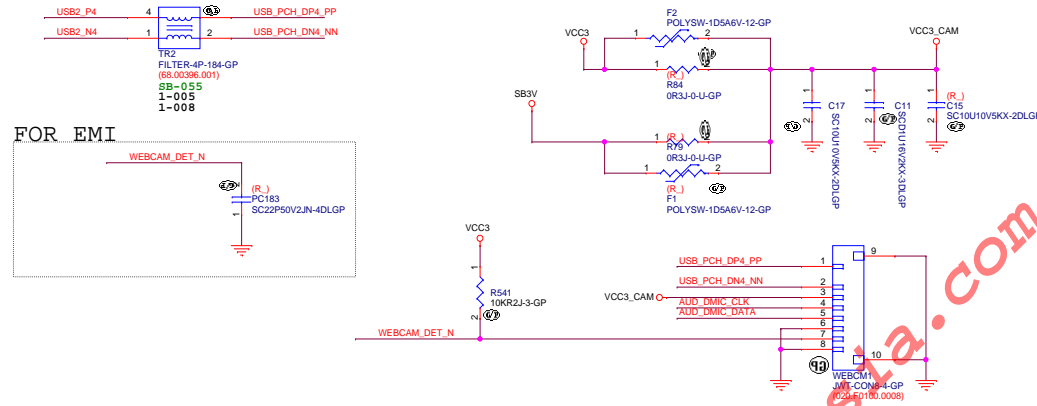
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>037_ USB Charger (RES)</b>			
Size A	Document Number <b>Rosa_KBL-U AIO</b>		Rev <b>SB</b>
Date: Thursday, June 23, 2016		Sheet 37 of	105

# WEBCAM

## WEBCAM

- 16 USB2\_N4
- 16 USB2\_P4
- 27 AUD\_DMIC\_CLK
- 27 AUD\_DMIC\_DATA
- 24 WEBCAM\_DET\_N



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Title: 038\_WEBCAM

Size: C Document Number: Rosa\_KBL-U AIO Rev: SB

Date: Thursday, June 23, 2016 Sheet: 38 of 105

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Title

**039\_ (Reserved)**

Size  
A

Document Number

**Rosa\_KBL-U AIO**

Rev

**SB**

Date: Thursday, June 23, 2016

Sheet 39 of 105

7,17,24,43,52,55 SLP\_S3\_N >> 2 1 R861 ORIGIN:BAR



«Core Design»



Size	Document Number
Custom	Rosa_KBL-U AIO

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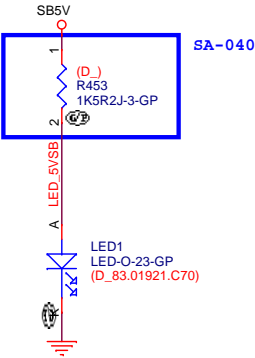
Rev  
SB



SB-040


SA-045  
SA-055

SB5V LED

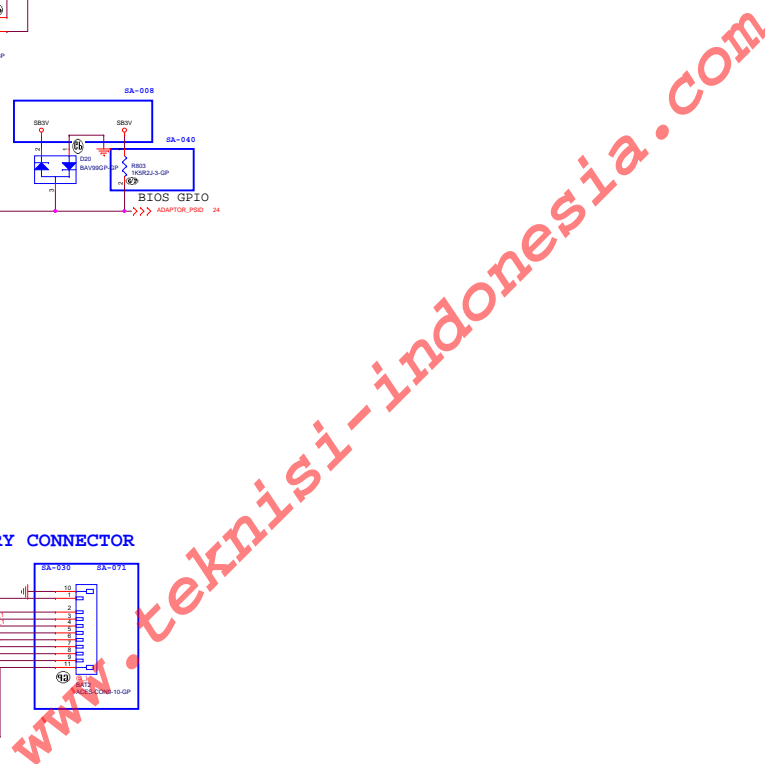


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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>041_DSW_POWER_CTL</b>			
Size B	Document Number <b>Rosa_KBL-U AIO</b>		Rev <b>SB</b>
Date:	Thursday, June 23, 2016	Sheet 41 of	105

### Adaptor in to generate DCBATOUT

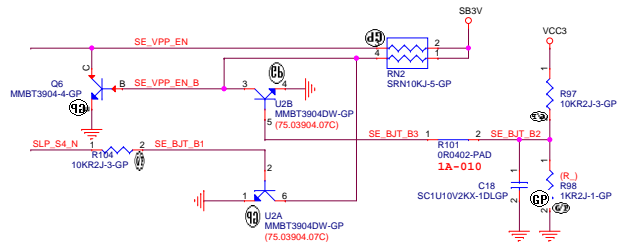


SA-009  
SA-016  
SA-061

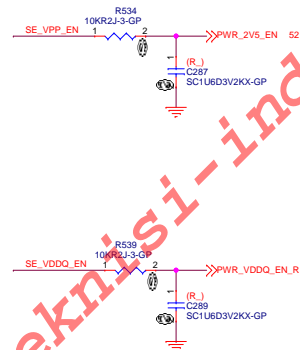
SA-009

## DDR4 Power Sequence

### VPP(2.5V) enable



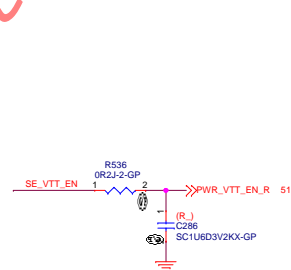
SA-061



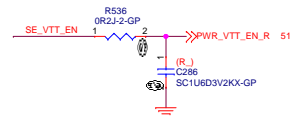
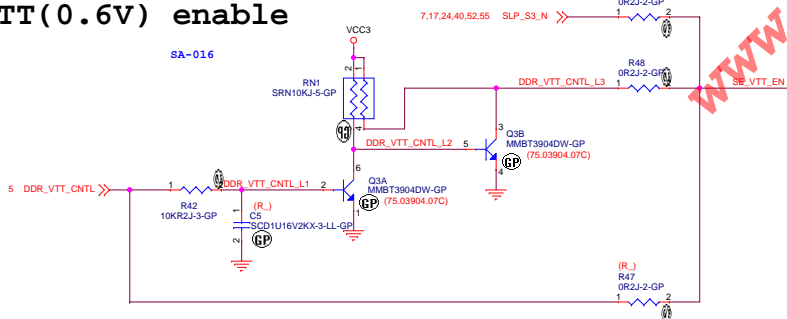
### VDDQ(1.2V) enable



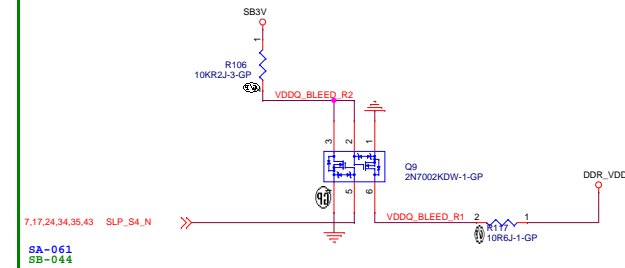
SA-061



### VTT(0.6V) enable



### VDDQ discharge

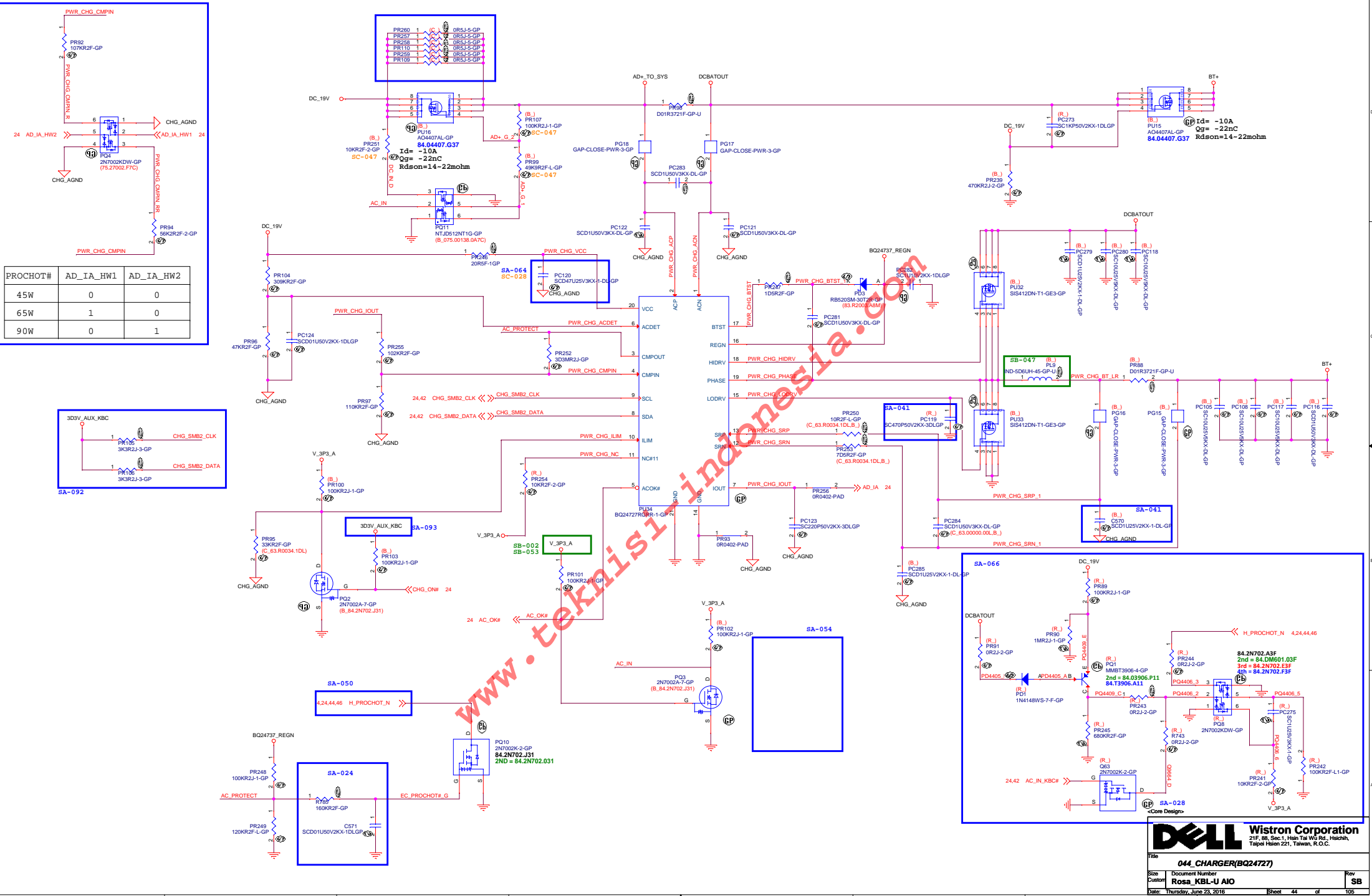


<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			043_DDR4 POWER EN & SEQ.
Size	Document Number	Rev	
Custom	Rosa_KBL-U AIO	SB	
Date:	Thursday, June 23, 2016	Sheet	43 of 105

PROCHOT#	AD_IA_HW1	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1



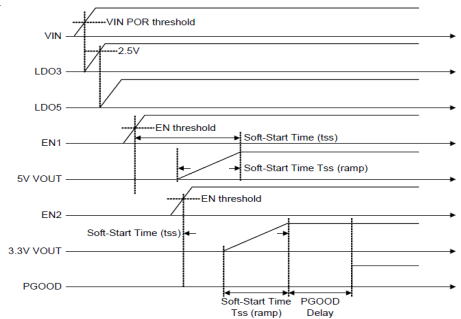
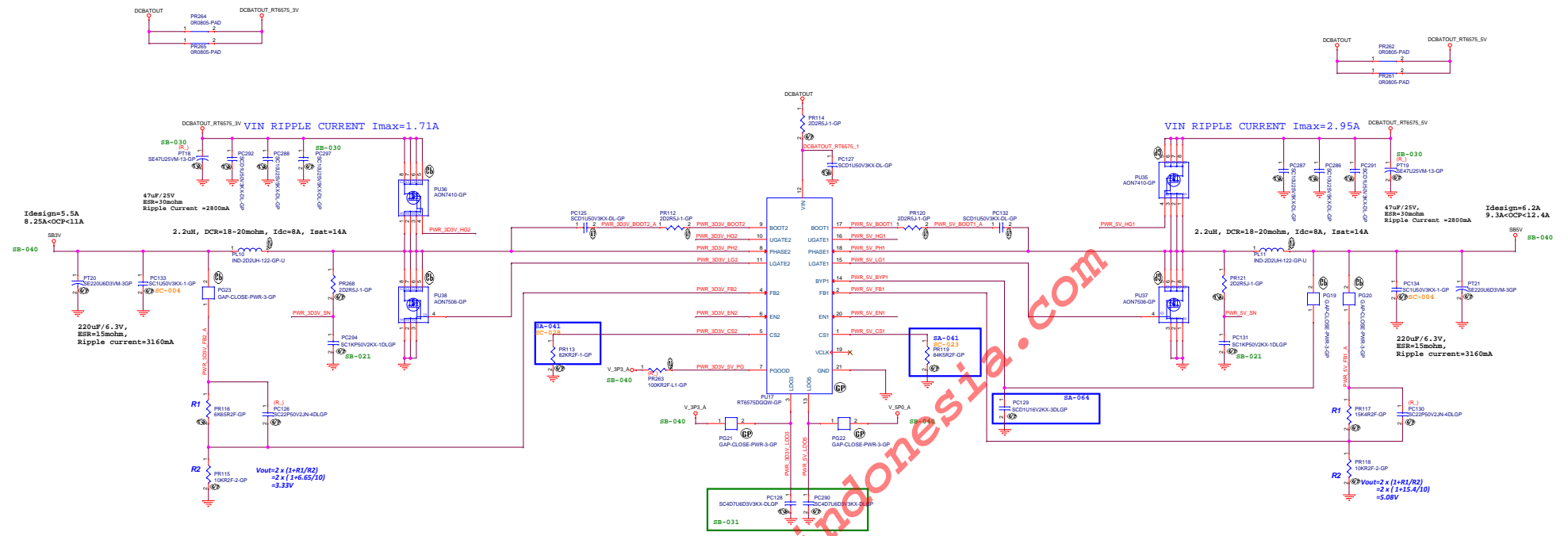
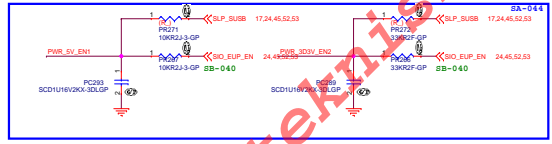
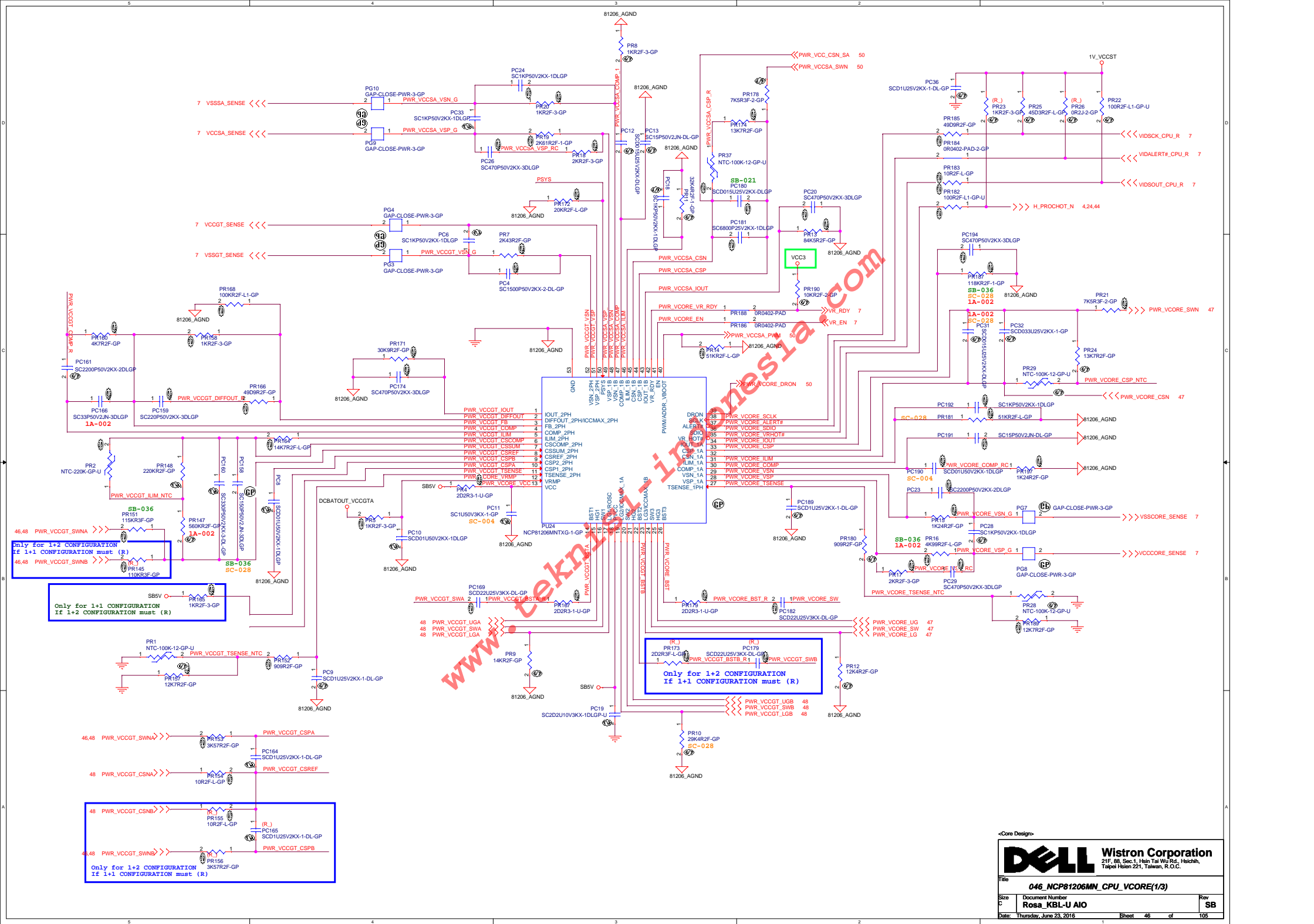
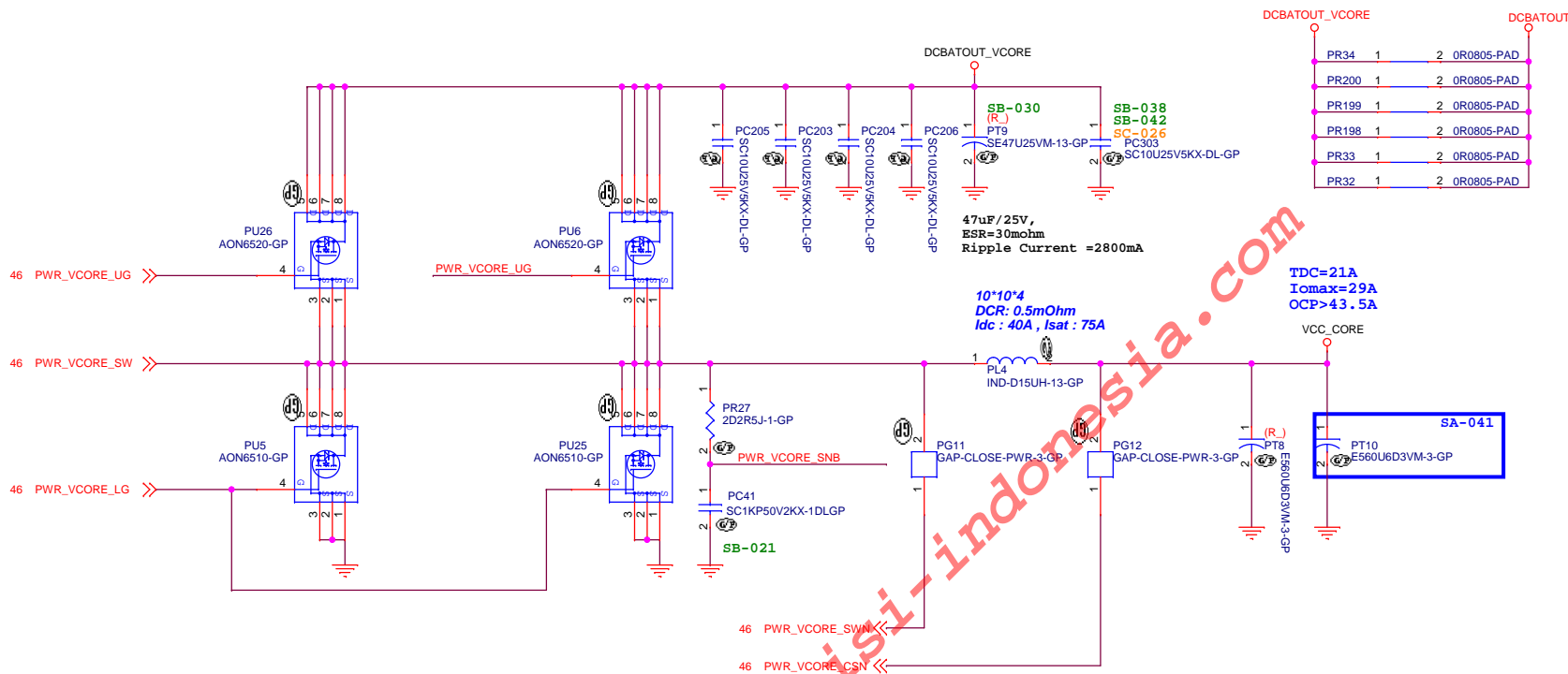


Figure 6. RT675B Timing



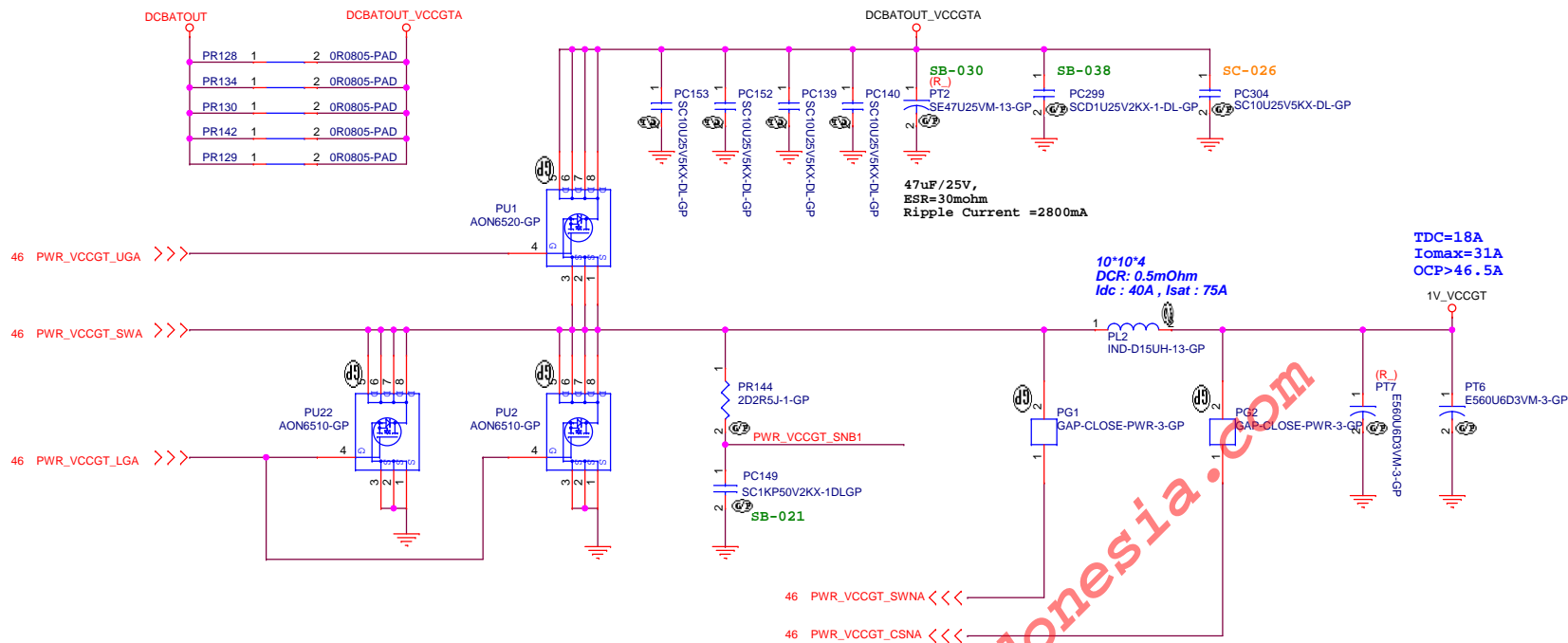
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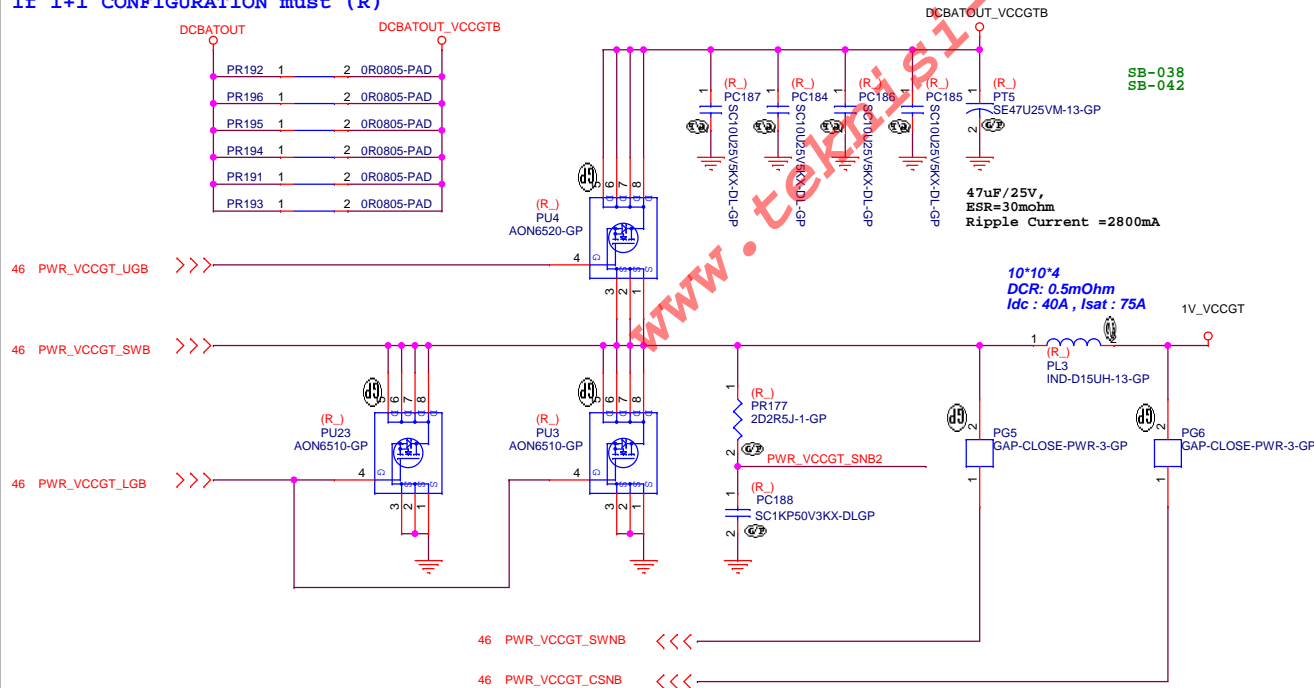


<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>047_NCP81206MN_CPU_VCORE(2/3)</b>	
Size A3	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>	
Date: Thursday, June 23, 2016		Sheet 47 of 105	



Only for 1+2 CONFIGURATION  
If 1+1 CONFIGURATION must (R)



<Core Design>



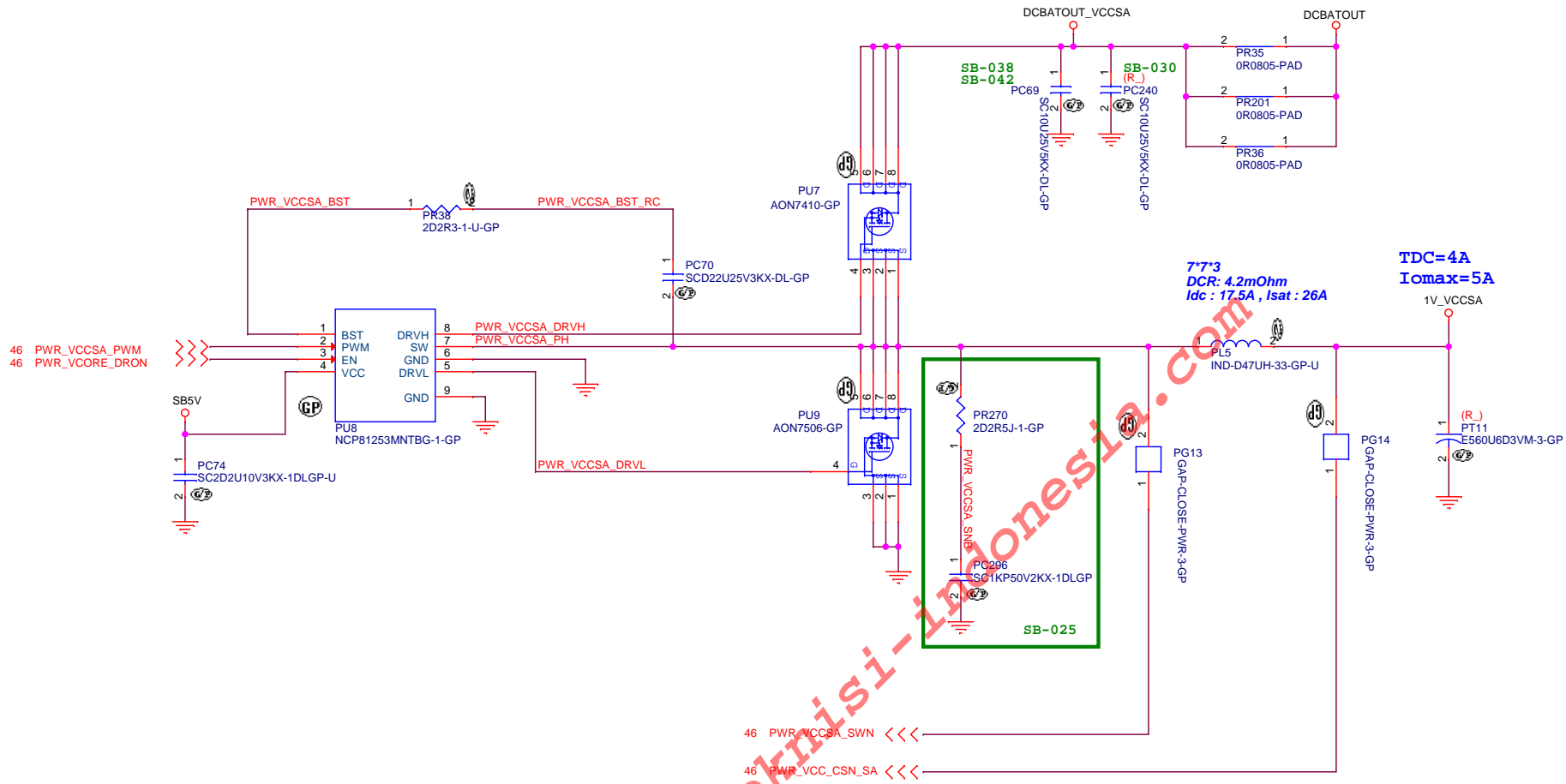
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>048_NCP81206MN_CPU_VCCGT(3/3)</b>		
Size A3	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016 Sheet 48 of 105		



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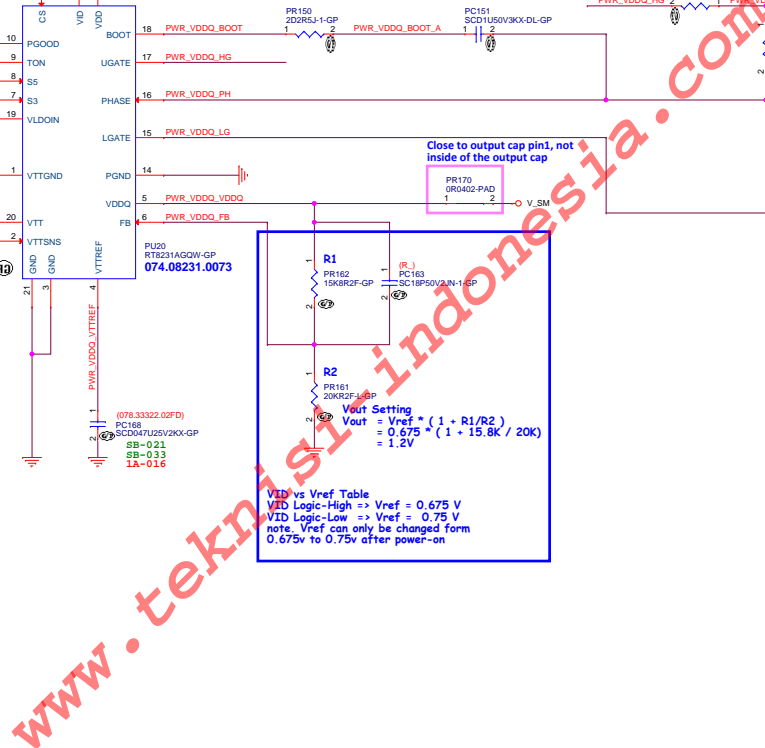
<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>050_NCP81253MN_CPU_VCCSA</b>		
Size B	Document Number <b>Rosa_KBL-U A10</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016	Sheet 50 of 105	

```
SSID = PWR.Plane.Regulator_1p2v0p6v
```



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

**RT8237 for 1D0V**



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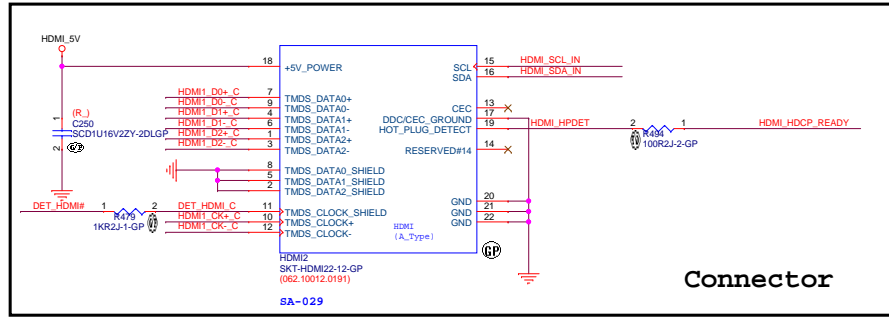
## HDMI - IN

### HDMI

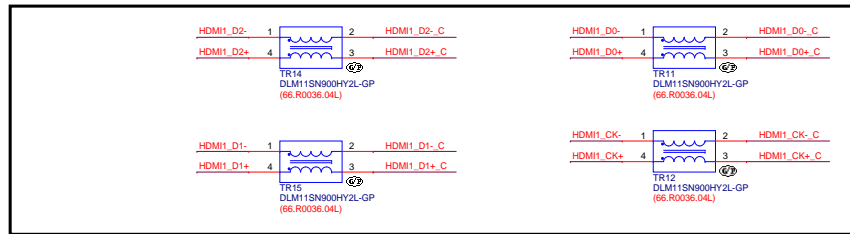
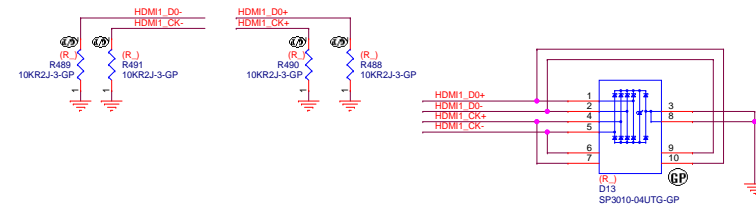
55 HDMI1\_D2+  
55 HDMI1\_D2-  
55 HDMI1\_D1+  
55 HDMI1\_D1-  
55 HDMI1\_D0+  
55 HDMI1\_D0-  
55 HDMI1\_CK+  
55 HDMI1\_CK-

24.55 DET\_HDMI#

55 DDC\_WP  
55 HDMI1\_SDA  
55 HDMI1\_SCL  
55 HDMI\_HDCP\_READY

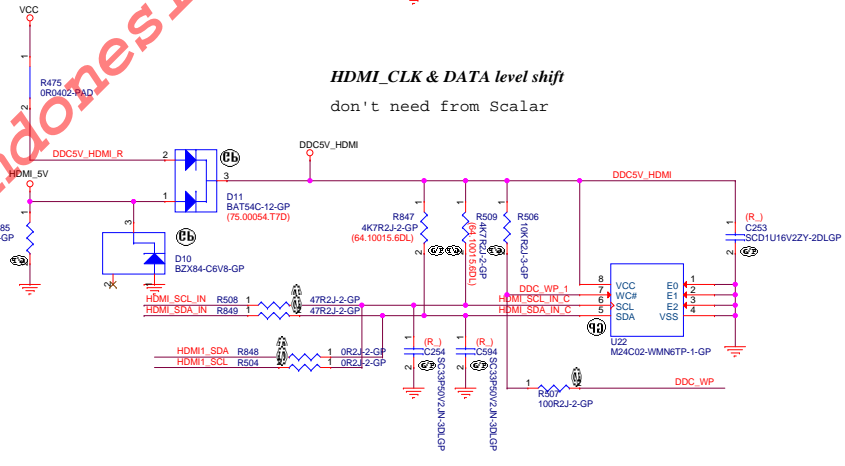


## EMI/ESD near Connector

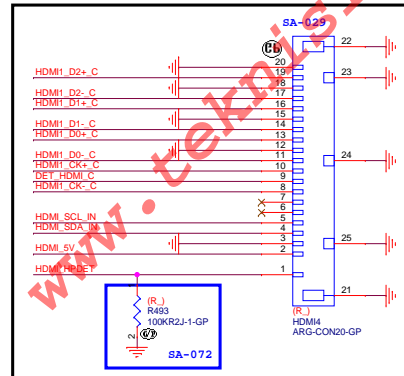
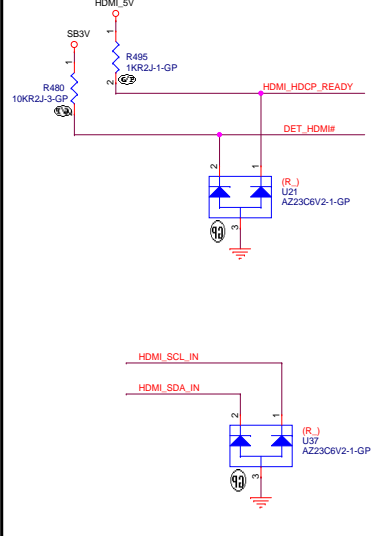


## HDMI\_CLK & DATA level shift

don't need from Scalar



## EMI/ESD near Connector



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Title: 056\_HDMI\_IN  
Size: C Document Number: Rosa\_KBL-U AIO Rev: SB  
Date: Thursday, June 23, 2016 Sheet: 56 of 105



## HDMI

## HDMI

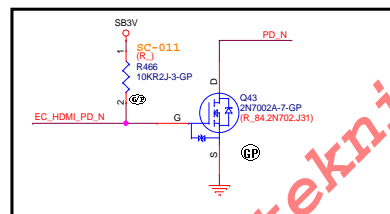
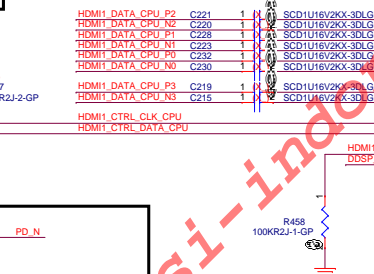
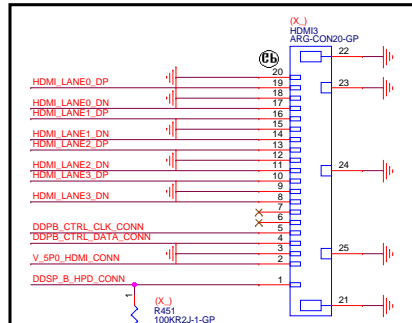
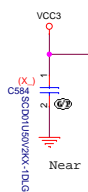
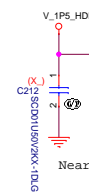
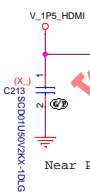
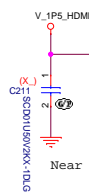
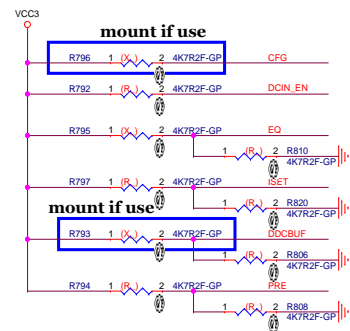
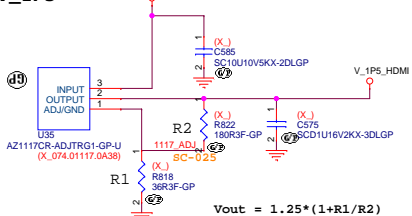
Need to add diode!!!

8 HDMI1\_DATA\_CPU\_P0  
8 HDMI1\_DATA\_CPU\_N0  
8 HDMI1\_DATA\_CPU\_P1  
8 HDMI1\_DATA\_CPU\_N1  
8 HDMI1\_DATA\_CPU\_P2  
8 HDMI1\_DATA\_CPU\_N2  
8 HDMI1\_DATA\_CPU\_P3  
8 HDMI1\_DATA\_CPU\_N3

8 HDMI1\_CTRL\_CLK\_CPU  
8 HDMI1\_CTRL\_DATA\_CPU  
8 HDMI1\_OUT\_HPD  
24 EC\_HDMI\_PD\_N

Reserved for HDMI re-Driver

## V\_1P5



## V\_1P5\_HDMI

## VCC3

## VDD33

## VDD33

## VDD33

## VDD33

## VDD33

## VDD33

## VDD33

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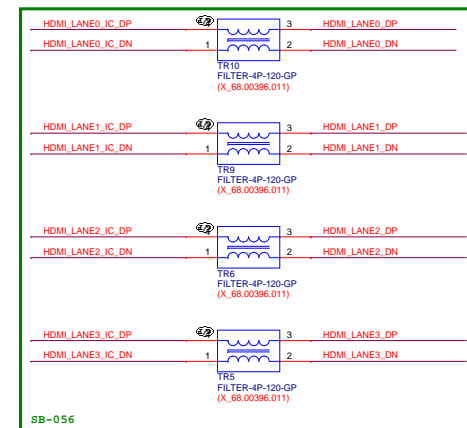
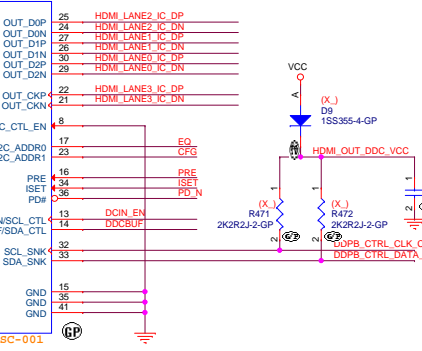
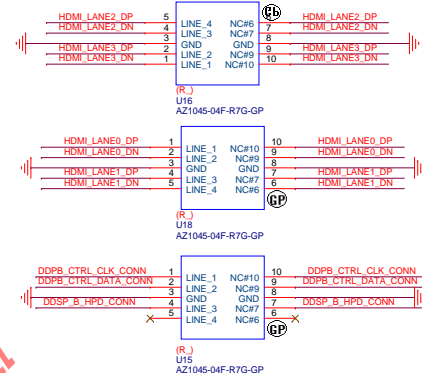
## VDD33

## VDD33

## VDD33

## VDD33

## ESD



&lt;Core Design&gt;

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Title

057\_HDMI\_OUT

Size

Document Number

Rosa\_KBL-U AIO

Date: Thursday, June 23, 2016

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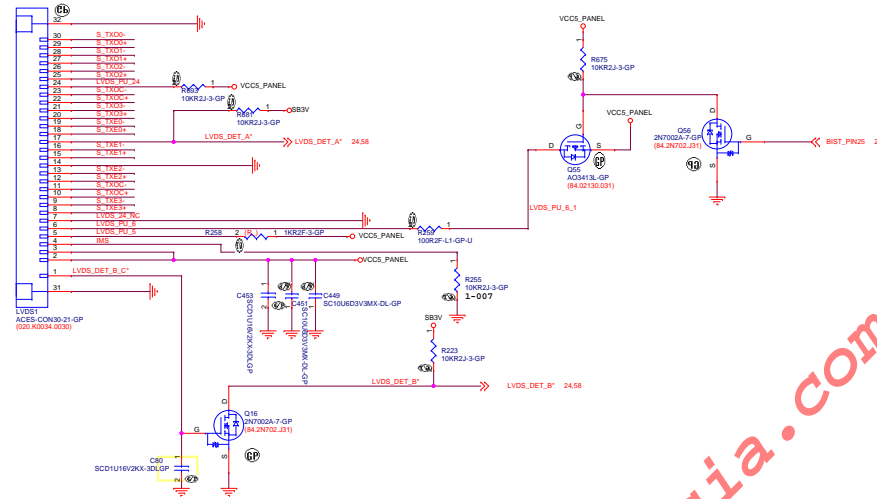
Rev

SB

8A-013  
8A-086  
8A-063



## LVDS1



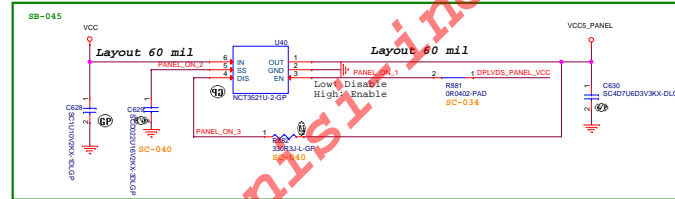
## From RTD2136S to LVDS

55 S\_TXE3+ S\_TXE3+  
55 S\_TXE3- S\_TXE3-  
55 S\_TXE2+ S\_TXE2+  
55 S\_TXE2- S\_TXE2-  
55 S\_TXE1+ S\_TXE1+  
55 S\_TXE1- S\_TXE1-  
55 S\_TXE0+ S\_TXE0+  
55 S\_TXE0- S\_TXE0-

55 S\_TX00+ S\_TX00+  
55 S\_TX00- S\_TX00-  
55 S\_TX01+ S\_TX01+  
55 S\_TX01- S\_TX01-  
55 S\_TX02+ S\_TX02+  
55 S\_TX02- S\_TX02-  
55 S\_TX03+ S\_TX03+  
55 S\_TX03- S\_TX03-  
55 S\_TX04+ S\_TX04+  
55 S\_TX04- S\_TX04-

## GPIO

24.58 LVDS\_DET\_A+ <<<  
24.58 LVDS\_DET\_B+ <<<  
55 DPLVDS\_PANEL\_VCC <<< DPLVDS\_PANEL\_VCC  
24.55 IMS <<<



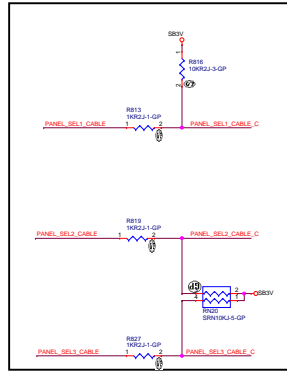
24.05 PANEL\_SEL1\_CABLE  
24.05 PANEL\_SEL2\_CABLE  
24.05 PANEL\_SEL3\_CABLE

55 DPLVDS\_PWMOUT  
55 DPLVDS\_PWMOUT

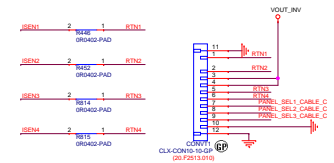
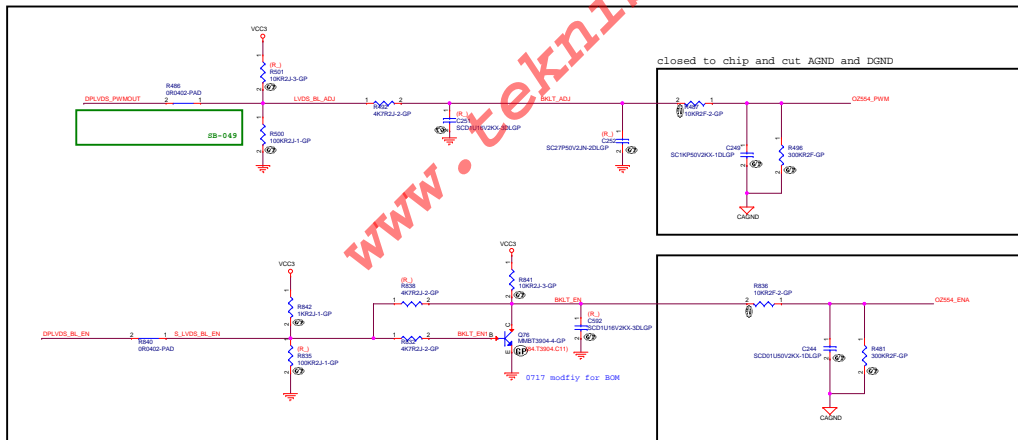
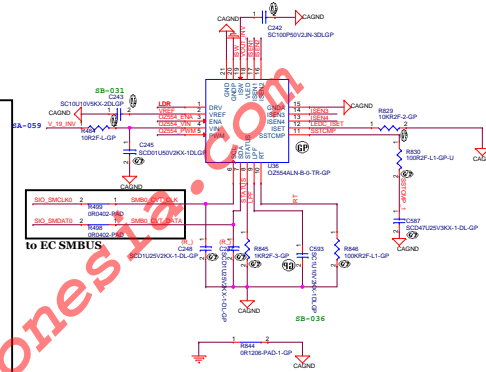
24.05 DPLVDS\_BL\_EN  
24.05 DPLVDS\_BL\_EN

24.79 SDO\_SMDAIO  
24.79 SDO\_SMDAIO

Cable detection			
PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Status
1	1	1	Panel unplug
X	X	X	Panel plug



Cable Spec				
23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout(pin number of CONV(T1))
LG	1	0	0	3.4 Vout 1.5.6 RTN
BOE	1	1	0	3.4 Vout 1.5.6 RTN
AUO	1	0	1	3.4 Vout 1.2.5.6 RTN
19.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout(pin number of CONV(T1))
AUO	0	1	0	3.4 Vout 1.6 RTN
INX	0	0	1	3.4 Vout 1.2.5.6 RTN
21.5"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout(pin number of panel)
LG	0	0	0	3.4 Vout 1.6 RTN
Samsung	0	1	1	2.3 Vout 1.4 RTN

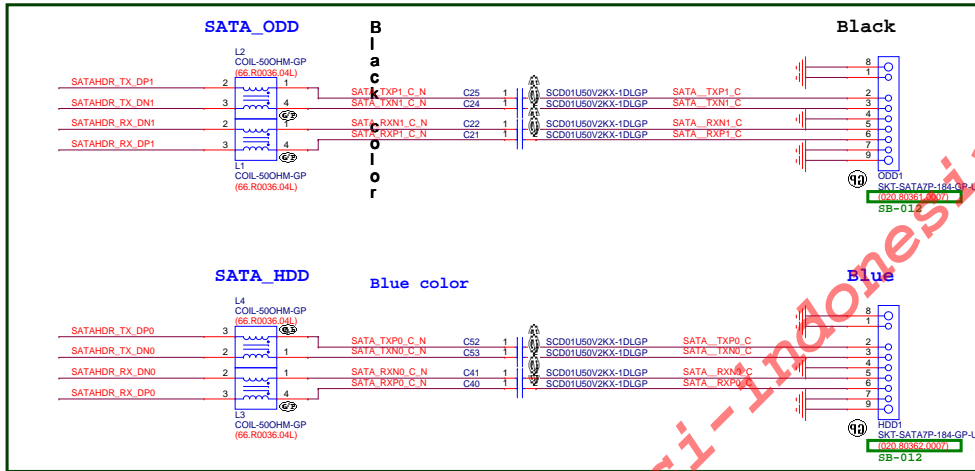
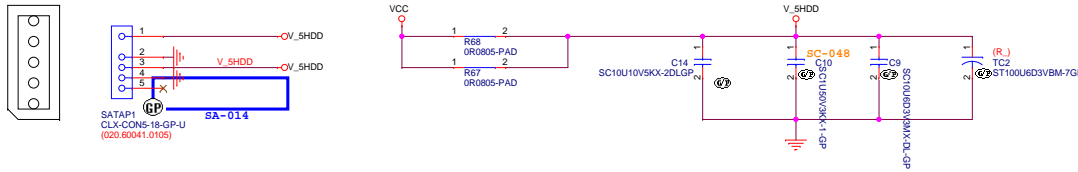


## SATA

- 16 SATAHDR\_RX\_DP0
- 16 SATAHDR\_RX\_DN0
- 16 SATAHDR\_TX\_DN0
- 16 SATAHDR\_TX\_DP0
- 16 SATAHDR\_RX\_DP1
- 16 SATAHDR\_RX\_DN1
- 16 SATAHDR\_TX\_DN1
- 16 SATAHDR\_TX\_DP1

## SATA

Layout: Please put them together



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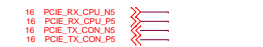
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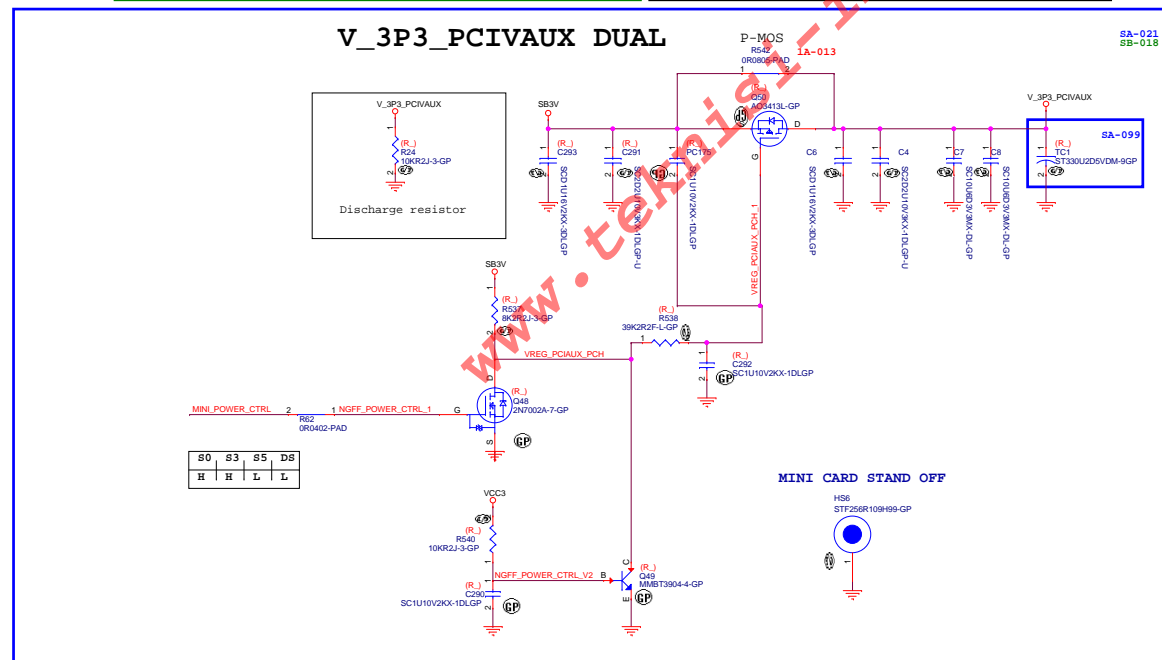
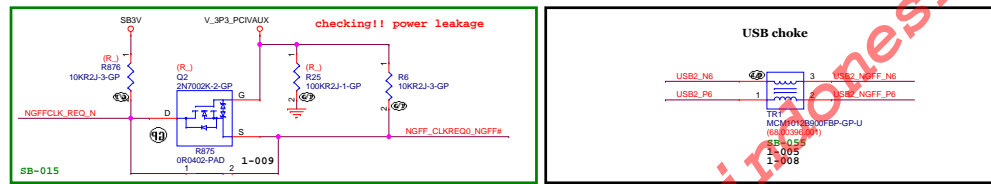
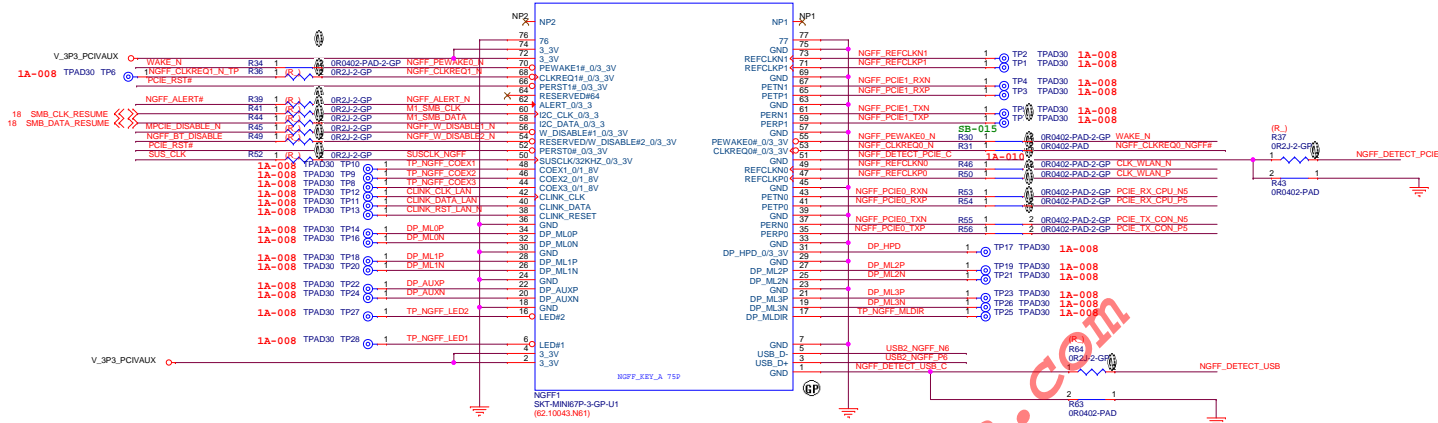
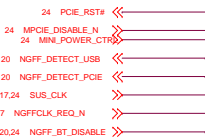
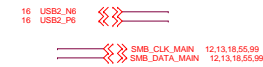
Title <b>060_HDD/ODD</b>		
Size C	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016 1 Sheet 60 of 105		

***NGFF(A Key)***

H: 4.2mm

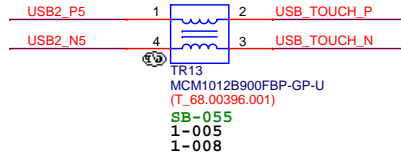
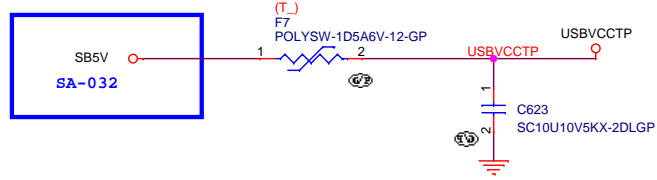


NGFF Card

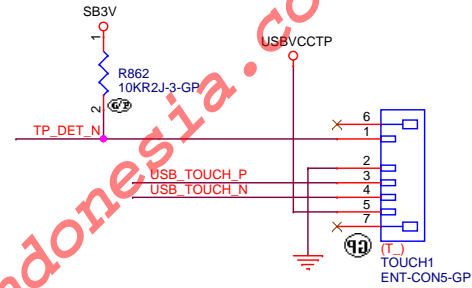
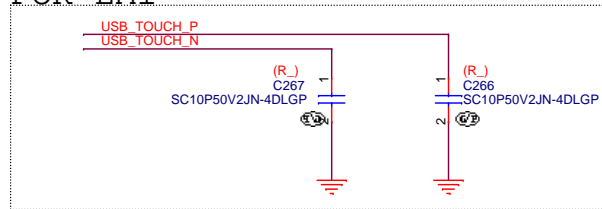


# USB TOUCH PANEL

## TOUCH PANEL



## FOR EMI



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Title <b>062_TOUCH</b>		
Size B	Document Number <b>Rosa_KBL-U A10</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016	Sheet 62 of 105	

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Title <b>063_ (Reserved)</b>		
Size A4	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016		Sheet 63 of 105

## Power Button/Reset

24 PWRBTN\_N << PWRBTN\_N

TO SIO

## HD\_LED

16 SATA\_LED\_N >>

24 SIO\_HDD\_LED >>

24 SIO\_YELLOW >>

24 SIO\_GREEN\_PWM <<

## OSD

18,24,55 OSD\_MENU << OSD\_MENU

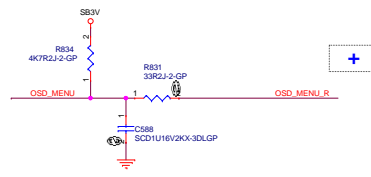
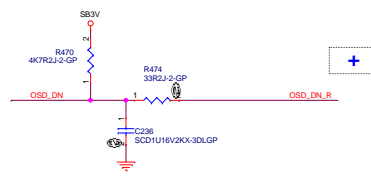
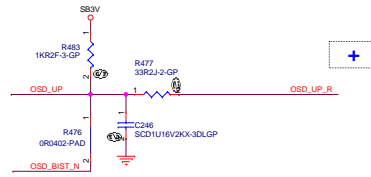
20,55 OSD\_UP << OSD\_UP

20,55 OSD\_DN << OSD\_DN

24,55 OSD\_BIST\_N << OSD\_BIST\_N

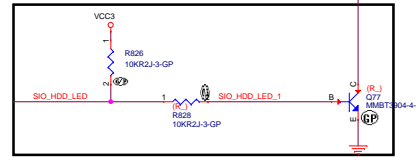
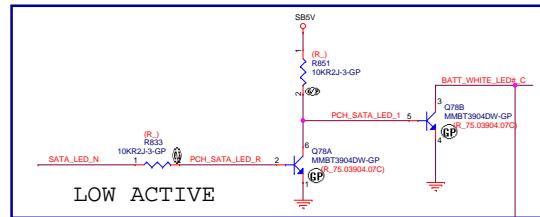
16 PWRCN\_DET\_N << PWRCN\_DET\_N

## OSD Buttons



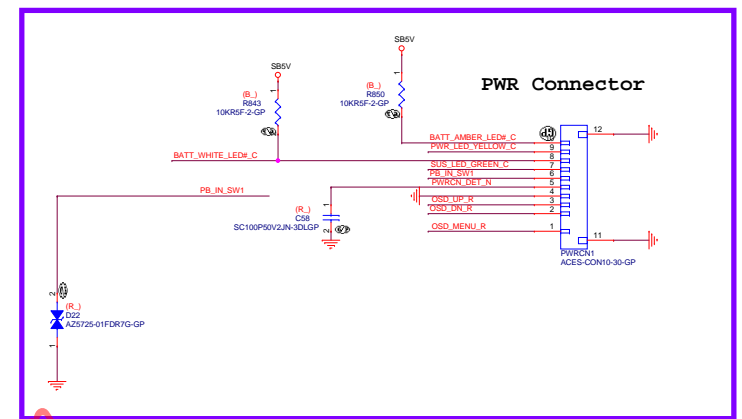
	Function
BTN1	UP
BTN2	DOWN
BTN3	Panel OFF

## HDD LED Circuit

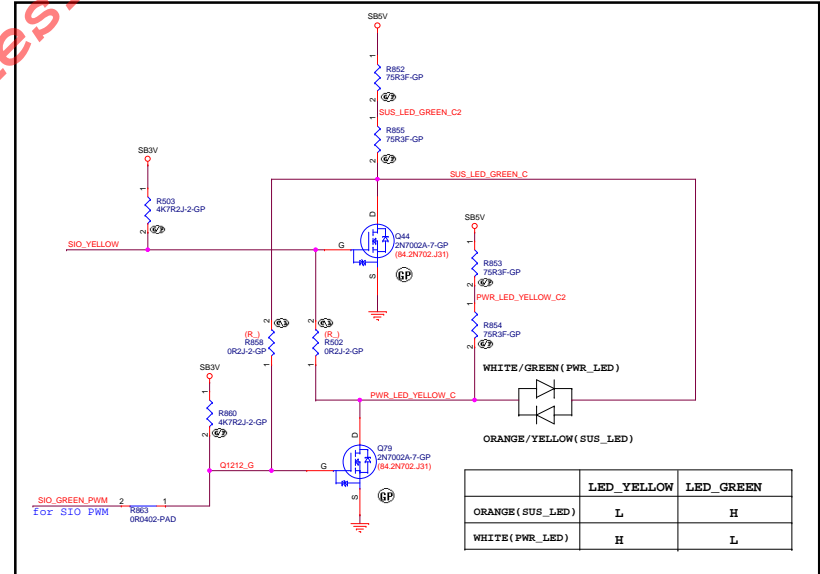


For Factory HDD LED Test

## PWR Connector



## Power LED Circuit



	LED_YELLOW	LED_GREEN
ORANGE (SUS_LED)	L	H
WHITE (PWR_LED)	H	L


<Core Design>



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<Core Design>

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Title <b>065_ (Reserved)</b>		
Size A4	Document Number <b>Rosa_KBL-U AIO</b>	Rev <b>SB</b>
Date: Thursday, June 23, 2016		Sheet 65 of 105

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Title

066\_(Reserved)

Size	Document Number	Rev
A3	Rosa_KBL-U AIO	SB

Date: Thursday, June 23, 2016

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# Free Fall Sensor

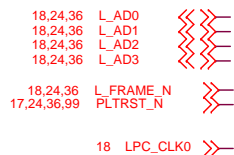
SA-014

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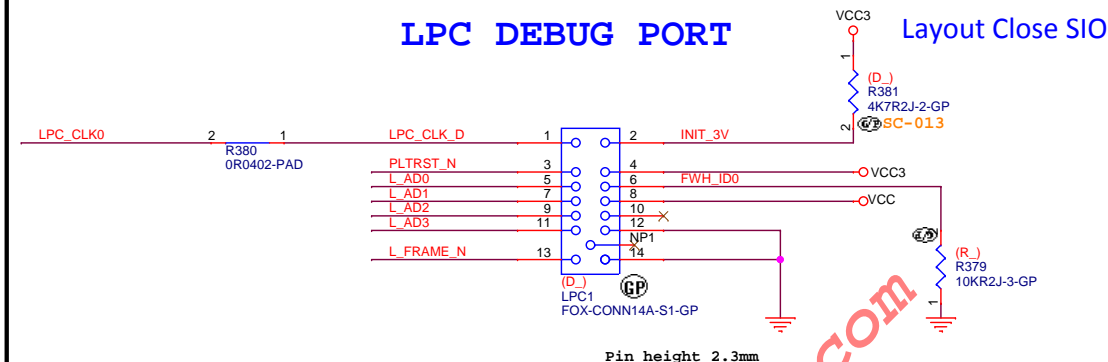
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Title <b>067_FFS(NEW)</b>			
Size A	Document Number <b>Rosa_KBL-U AIO</b>		Rev <b>SB</b>
Date: Thursday, June 23, 2016		Sheet 67 of	105

# LPC DEBUG PORT



# LPC DEBUG PORT



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068_DEBUG/HDT		
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Title

**069\_ (Reserved)**

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A

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072\_ (Reserved)

Size

A3

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## PCIEX4

24,76 PLTRST\_SL\_N >>  
79 PEX\_RST\_GPU <<

16 PEG\_TXP0 >>  
16 PEG\_TXN0 >>

16 PEG\_TXP1 >>  
16 PEG\_TXN1 >>

16 PEG\_TXP2 >>  
16 PEG\_TXN2 >>

16 PEG\_TXP3 >>  
16 PEG\_TXN3 >>

16 PEG\_RXP0 >>  
16 PEG\_RXN0 >>

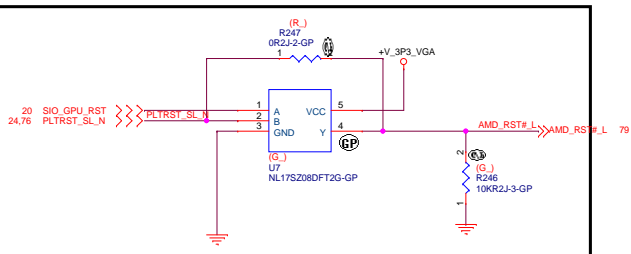
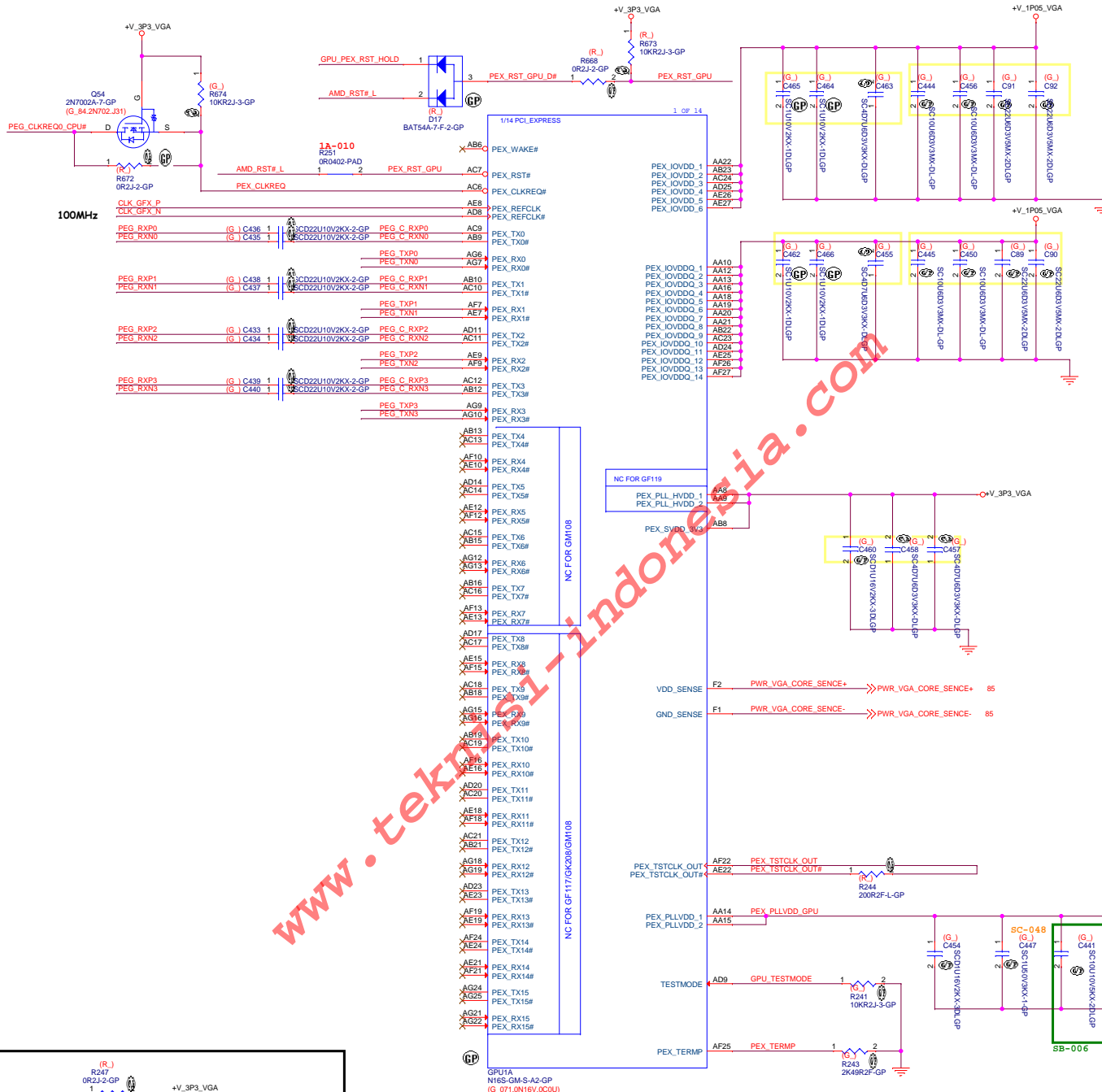
16 PEG\_RXP1 >>  
16 PEG\_RXN1 >>

16 PEG\_RXP2 >>  
16 PEG\_RXN2 >>

16 PEG\_RXP3 >>  
16 PEG\_RXN3 >>

17 CLK\_GFX\_P >>  
17 CLK\_GFX\_N >>

17 PEG\_CLKREQ0\_CPU# <<  
79 GPU\_PEX\_RST\_HOLD >>



1U Under GPU

4.7U NEAR TO GPU

10U mid TO GPU

Michael 2011/12/12

Add two 1uF Caps according to the NV Comment

&lt;Core Design&gt;

**DELL** Wistron Corporation  
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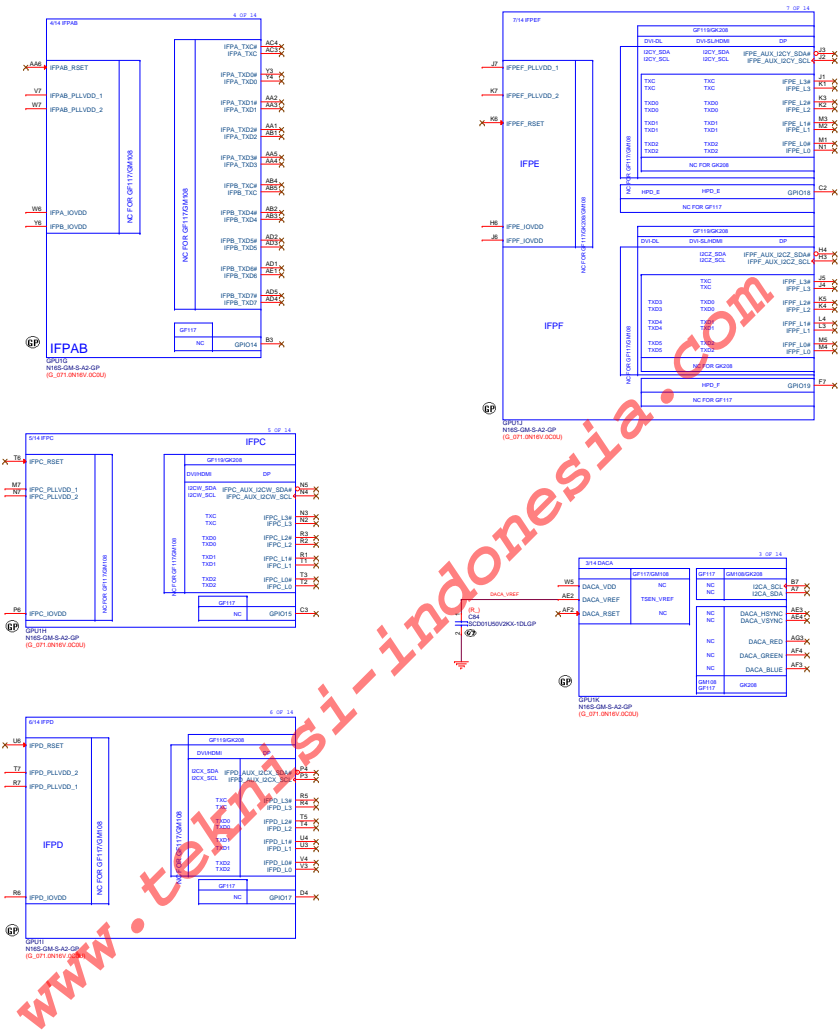
Title  
**076\_GPU(1/5) PEG**

Size  
**C** Document Number  
**Rosa\_KBL-U AIO**

Date: Thursday, June 23, 2016

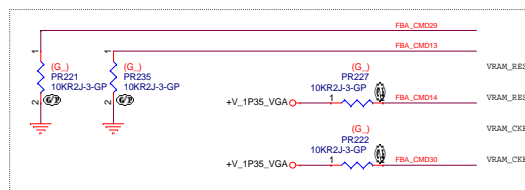
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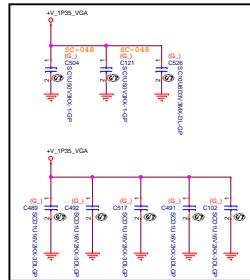
	<0...31	>32...63	MEMORY
12	28		RAS*
15	31		CAS*
5	21		WE*
0	16		CS*
8	24		AB1*
10	26		A0_A10
11	27		A1_A9
2	18		A2_BA0
1	17		A3_BA3
3	19		A4_BA2
4	20		A5_BA1
7	23		A6_A11
6	22		A7_A8
9	25		A12_RFU
13	29		RESET*
14	30		CKE*

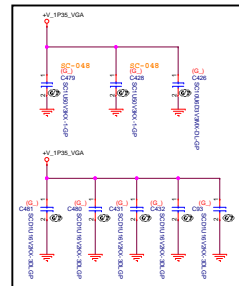












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SA-046\_whole page

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**083\_ (Reserved)**

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5

4

3

2

1

D

D

C

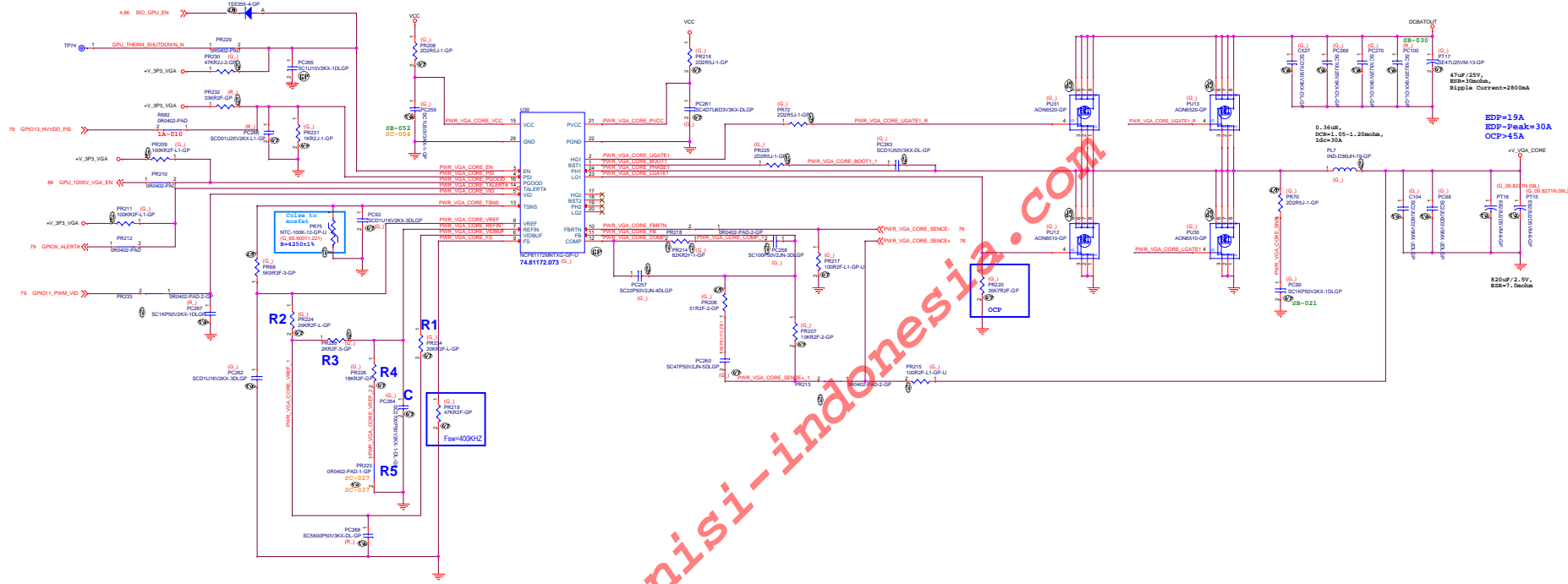
C

B

B

A

A



		Config A	Config B
R1 (1%)	KΩ	39	20
R2 (1%)	KΩ	39	20
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

5

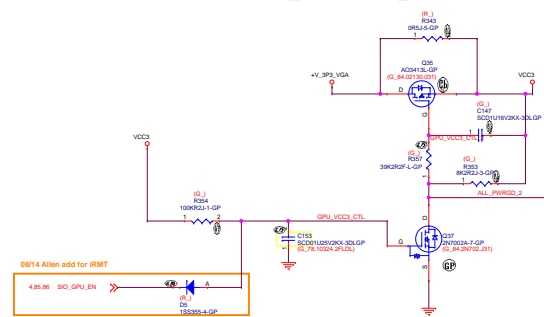
4

3

2

1

### 3D3V\_S0 to 3D3V\_DELAY Transfer

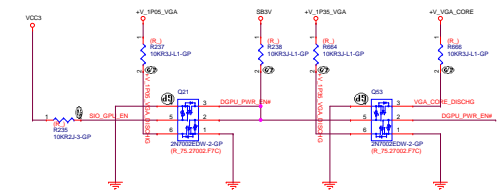
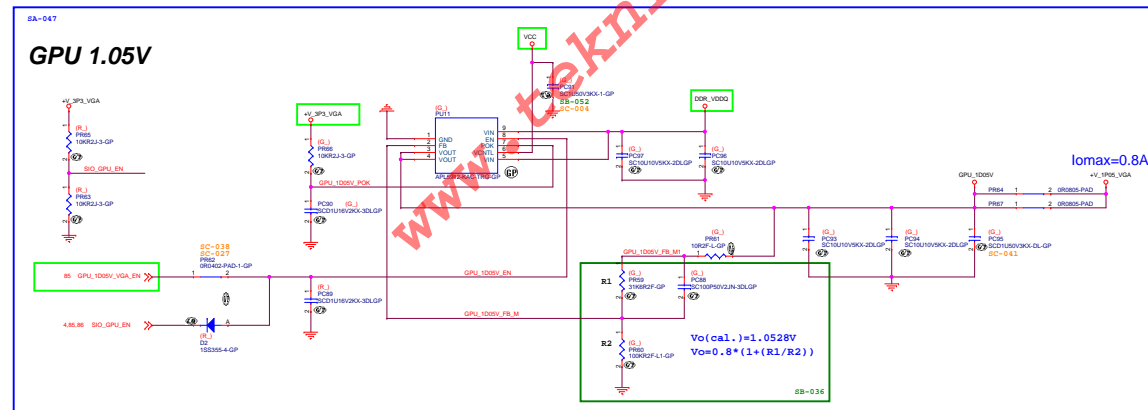
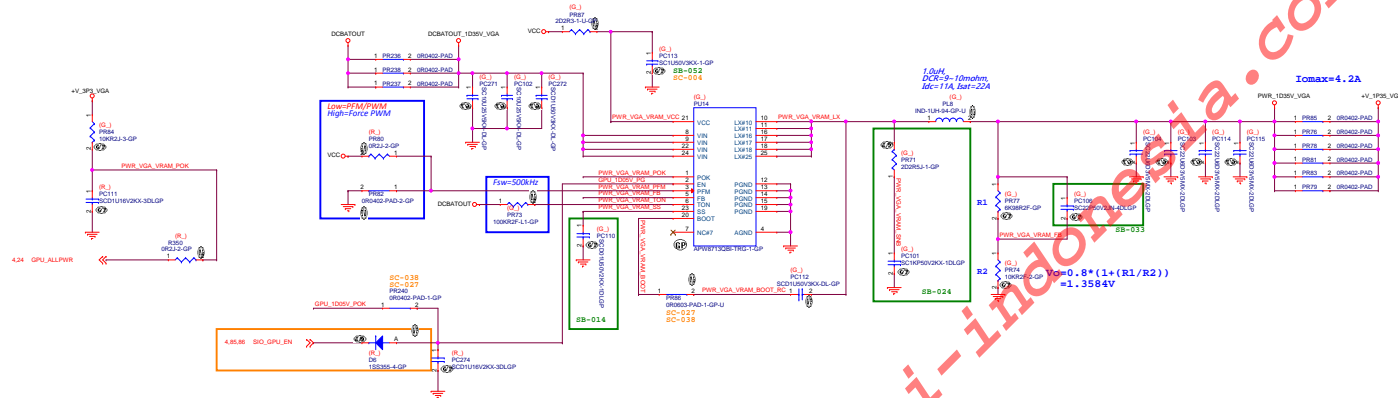


### Power Sequencing Requirement

GC6 2.0 requires the following power sequences. At GPU power up, first, the 3.3V power rails ramp up, followed by NVVDD then PEX\_VDD and all other 1.05V/1.0V power rails. And finally FBVDD/Q should power on. The following representation describes the required power sequencing for the GC6 2.0 system:

- ▶ Cold boot/Optimus: 3V3\_AON & 3V3\_MAIN → NVVDD → PEX\_VDD → FBVDD/Q
- ▶ GC6 2.0 Exit: 3.3V\_MAIN → NVVDD → PEX\_VDD

3.3->core->1.05->1.35



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Layout Note:  
ROUTE WITH MINIMAL STUB WITH RESPECT TO CPG<0>

Layout Note:  
ROUTE WITH MINIMAL STUB WITH RESPECT TO CPG<3>

17.24 RMBSST\_N >>> R2 1 2 100M2-1-GP SC-015

17.25 VCCST\_QD\_RN >>> R3 1 2 100M2-1-GP RMBSST\_PWDKX XDP

17.24 PM\_PVRNTH\_N <<< R4 2 1 00M2-PAD BP\_PWDKX\_RSTW

17.24 SYS\_PWDKX <<< R7 1 2 100M2-2-GP XDP SYS\_PWDKX

15 SPL\_R\_XDP <<< R1 2 1 100M2-3-GP SC-015

15.13.18.05 SMB\_DATA\_MASTER >>> R25 2 1 00M2-PAD XDP SMBDATA

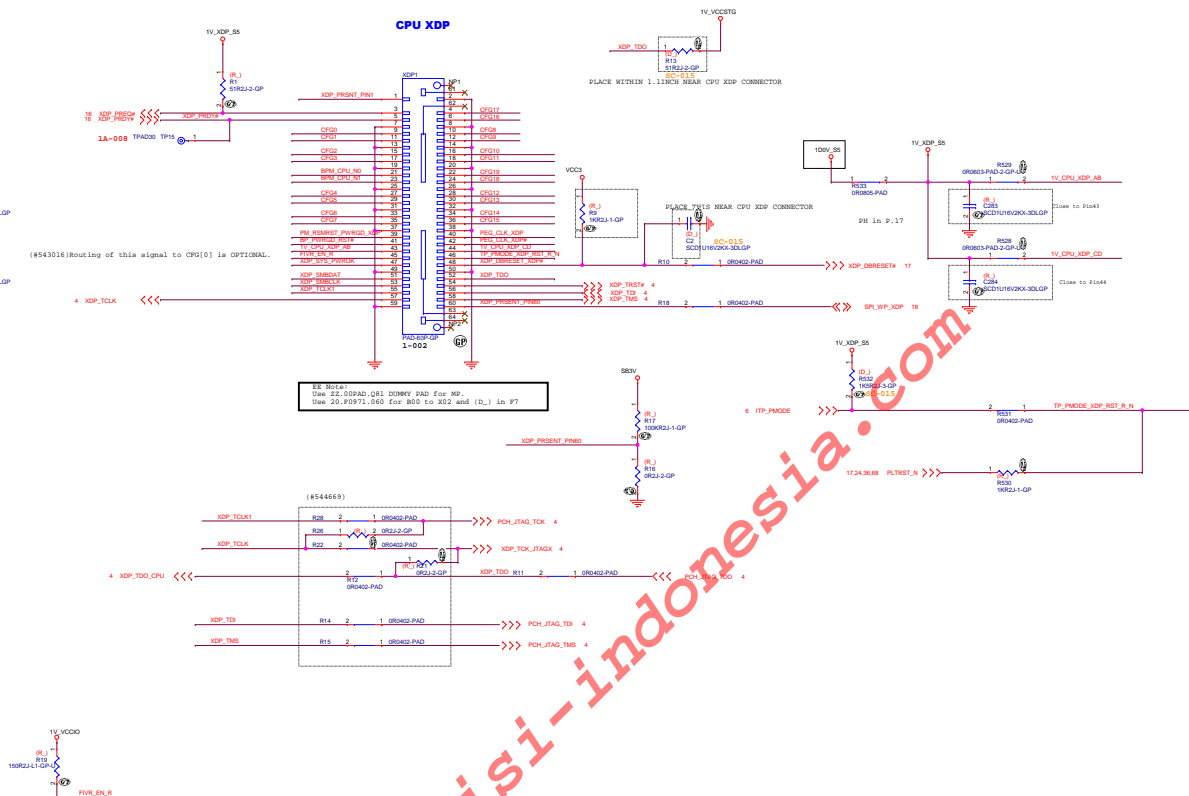
15.13.18.05 SMB\_CLK\_MASTER >>> R26 2 1 00M2-PAD XDP SMBCLK

17 PEG\_CLK\_CPU >>> R7 2 1 00M2-PAD PEG\_CLK\_XDP

17 PEG\_CLK\_CPUW >>> R8 2 1 00M2-PAD PEG\_CLK\_XDPW

6 CPG16H <<< CPG16S


4 BPG\_CPU\_N16 <<< BPG\_CPU\_N16S



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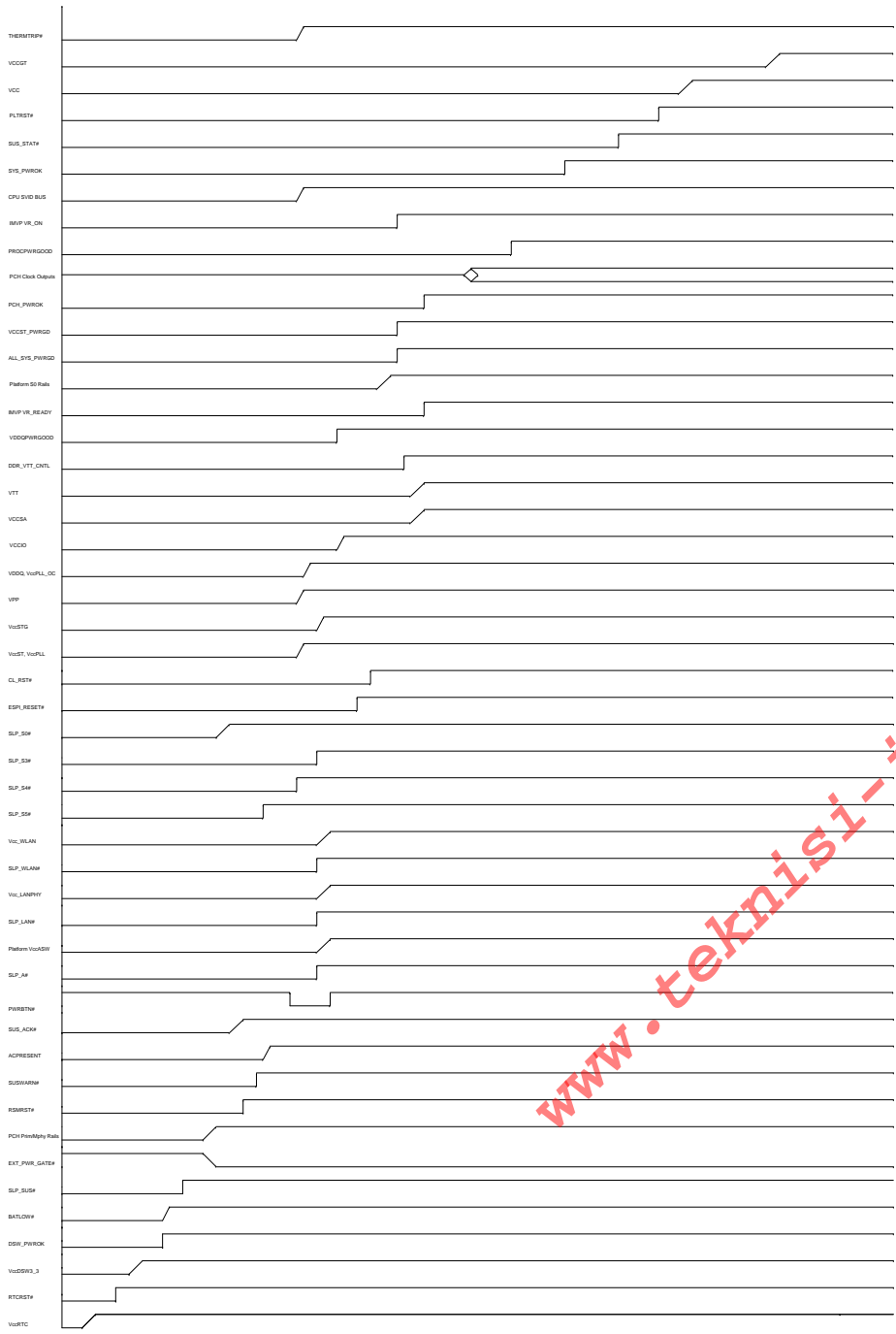
# 6-1.2-7c(2.40) stack up and impedance

叠层編號	6-1.2-7c	注意事項	1. Impedance Control tolerance $\pm 10\%$
完成板厚 (mm)	1.2 $\pm$ 0.12		2. Coupon 製作方式及 Impedance report 請依照 Wistron 規範製作

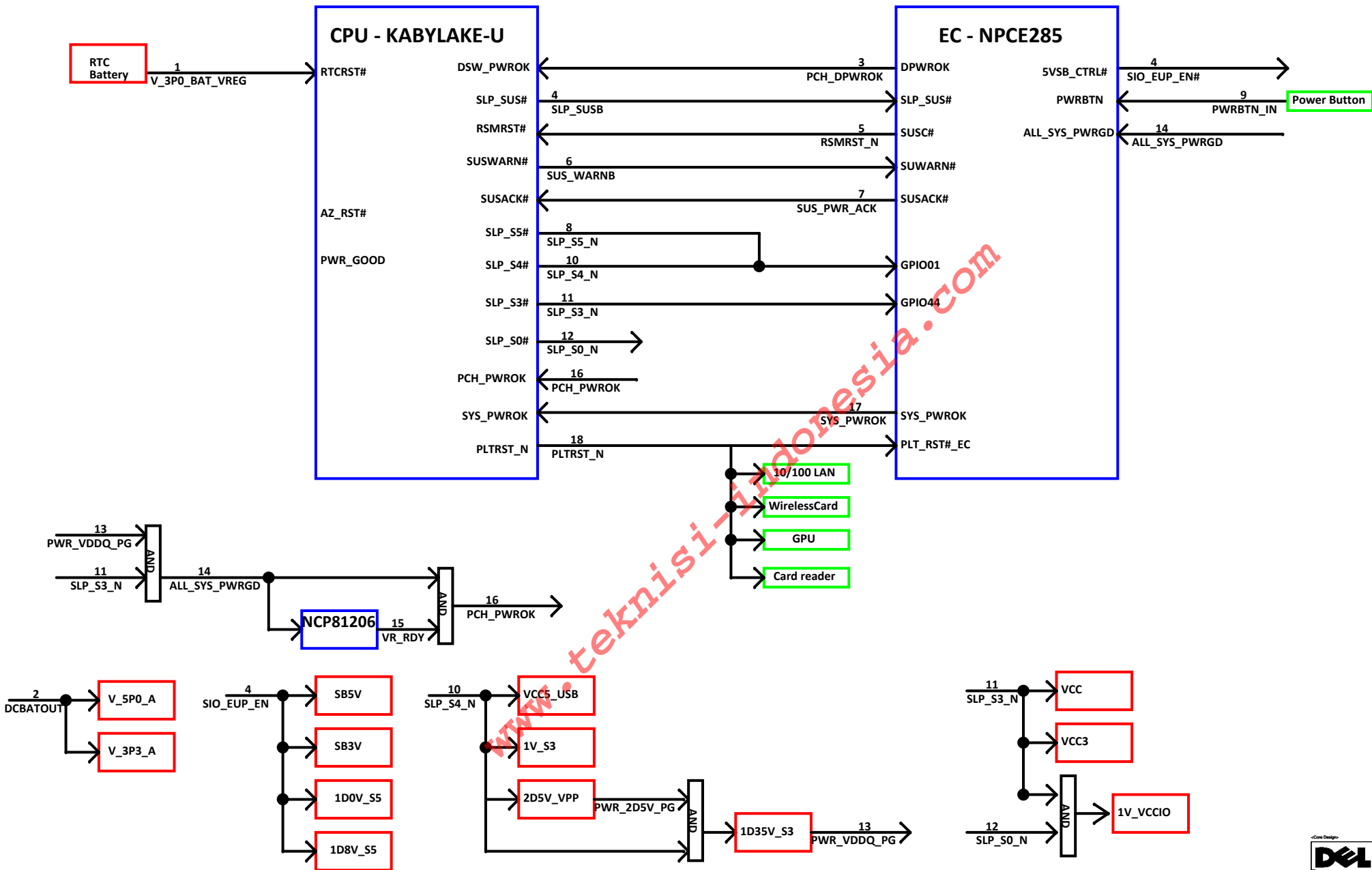
Stack up			Impedance Request List				
Layer	Spec	Thickness (mil)	Single Ended Type (Trace width : mil)				
			L1 (Ref. Plane) <sup>※ 1</sup>	L3 (Ref. Plane)	L4 (Ref. Plane)	L6 (Ref. Plane)	
L1	TOP		27.4 $\Omega$	12.0 (L2)	16.0 (L2/L5)	12.0 (L5)	
	PP	1.7	33 $\Omega$	9.0 (L2)	12.0 (L2/L5)	9.0 (L5)	
L2	GP <sup>※ 3</sup>	2.7	34 $\Omega$	8.5 (L2)	11.5 (L2/L5)	8.5 (L5)	
	Core	1.2	35 $\Omega$	8.0 (L2)	10.5 (L2/L5)	8.0 (L5)	
		4	37.5 $\Omega$	7.0 (L2)	9.5 (L2/L5)	7.0 (L5)	
L3	Signal	1.2	39 $\Omega$	6.5 (L2) <sup>※ 4</sup>	9.0 (L2/L5)	6.5 (L5) <sup>※ 4</sup>	
	PP	24	40 $\Omega$	6.5 (L2) <sup>※ 4</sup>	8.5 (L2/L5)	6.5 (L5) <sup>※ 4</sup>	
L4	Signal	1.2	42 $\Omega$	5.5 (L2)	7.5 (L2/L5)	5.5 (L5)	
	Core	4	45 $\Omega$	5.0 (L2)	6.5 (L2/L5)	5.0 (L5)	
L5	GP	1.2	48 $\Omega$	4.5 (L2)	5.5 (L2/L5)	4.5 (L5)	
	PP	2.7	50 $\Omega$	4.0 (L2)	5.0 (L2/L5)	4.0 (L5)	
L6	Bottom	1.7	52 $\Omega$	3.5 (L2) <sup>※ 2</sup>	4.5 (L2/L5)	3.5 (L5) <sup>※ 2</sup>	
			55 $\Omega$	NA	4.0 (L2/L5)	NA	
Differential Type (Trace width/Space width/Trace width: mil)							
110 $\Omega$	NA	3.5/13/3.5 (L2/L5)	3.5/13/3.5 (L2/L5)	NA			
100 $\Omega$	3.5/10/3.5 (L2)	4/9/4 (L2/L5)	4/9/4 (L2/L5)	3.5/10/3.5 (L5)			
95 $\Omega$	3.5/6/3.5 (L2); 4/10/4 (L2)	4/6/4 (L2/L5)	4/6/4 (L2/L5)	3.5/6/3.5 (L5); 4/10/4 (L5)			
93 $\Omega$	3.5/5/3.5 (L2); 4/8/4 (L2)	4/5/4 (L2/L5); 5/9/5 (L2/L5)	4/5/4 (L2/L5); 5/9/5 (L2/L5)	3.5/5/3.5 (L5); 4/8/4 (L5)			
90 $\Omega$	4/6/4 (L2)	4/5/4 (L2/L5); 5/8/5 (L2/L5)	4/5/4 (L2/L5); 5/8/5 (L2/L5)	4/6/4 (L5)			
85 $\Omega$	4/4.5/4 (L2); 5/8/5 (L2)	5/5/5 (L2/L5); 5/5/5 (L2/L5)	5/5/5 (L2/L5); 5/5/5 (L2/L5)	4/4.5/4 (L5); 5/8/5 (L5)			
80 $\Omega$	5/5/5 (L2)	6/6/6 (L2/L5)	6/6/6 (L2/L5)	5/5/5 (L5)			
75 $\Omega$	6/6/6 (L2)	7/6/7 (L2/L5)	7/6/7 (L2/L5)	6/6/6 (L5)			
72 $\Omega$	7/8/7 (L2)	7/5/7 (L2/L5)	7/5/7 (L2/L5)	7/8/7 (L5)			
70 $\Omega$	7/6/7 (L2)	8/6/8 (L2/L5)	8/6/8 (L2/L5)	7/6/7 (L5)			
68 $\Omega$	6.5/4/6.5 (L2)	7.5/4/7.5 (L2/L5)	7.5/4/7.5 (L2/L5)	6.5/4/6.5 (L5)			
65 $\Omega$	8/6/8 (L2)	9/5/9 (L2/L5)	9/5/9 (L2/L5)	8/6/8 (L5)			
Remark:							
※ 1: "Ref. Plane" means the reference plane of the traces.							
※ 2: Trace space should be wider than 4.0mil (Wistron internal only).							
※ 3: G is GND, P is PWR							
※ 4: Only choose one signal type and on layer L1&L6							
Total	45.6						

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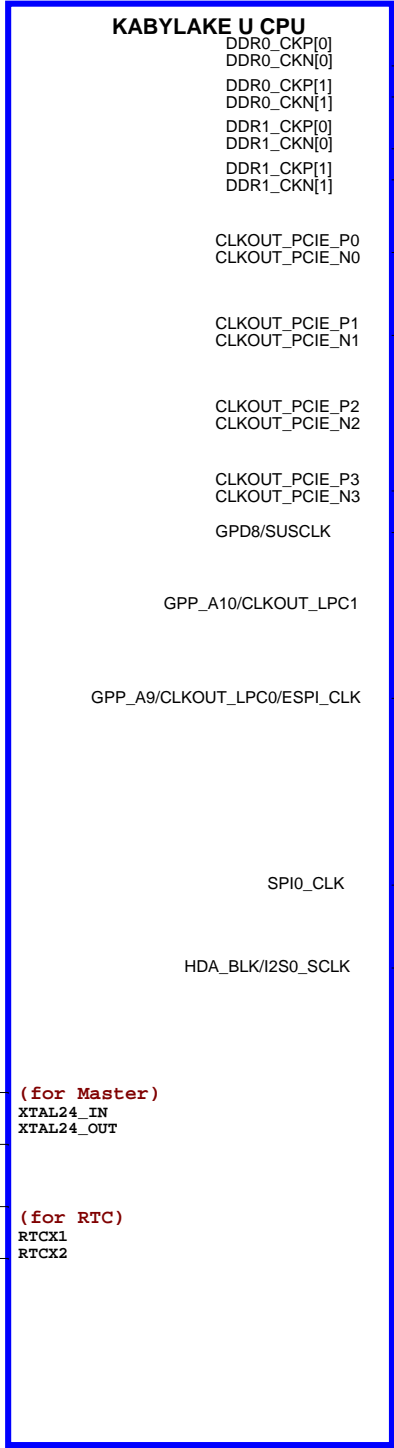
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Title			
<b>101_PCB STACKUP</b>			
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M\_A\_CLK0/M\_A\_CLK#0

M\_A\_CLK1/M\_A\_CLK#1

M\_B\_CLK0/M\_B\_CLK#0

M\_B\_CLK1/M\_B\_CLK#1

CLK\_GFX\_P/CLK\_GFX\_N  
100MHz

CLK\_GLAN\_P/CLK\_GLAN\_N  
100MHz

CLK\_WLAN\_P/CLK\_WLAN\_N  
100MHz

CLK\_CR\_P/CLK\_CR\_N  
100MHz  
SUS\_CLK

LPC\_CLK0  
33MHz

SPI\_CLK  
24MHz/48MHz/100MHz

AUD\_LINK\_BCLK

DIMM1

DIMM2

GPU(AMD EXO)

LAN RTL8106

NGFF A-key WLAN+BT

CARD READER  
RTS5227S

EC - NPCE285

LPC DEBUG PORT

SPI ROM

AUDIO ALC3661

SCALAR  
RTD2506S

X9505  
27MHz

X4  
25MHz

X9502  
14.31818MHz

X9503  
24MHz  
(for Master)  
XTAL24\_IN  
XTAL24\_OUT

X9504  
32.768KHz  
(for RTC)  
RTCX1  
RTCX2